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46	POWER INPUT&EMI CAP
47	PCB/MECHANICAL PARTS
48	+VCORE +VCCGT CONTROLLER
49	+VCORE PHASE 1&2
50	+VCORE PHASE 3
51	+VCCGT PHASE 1&2
52	+VCCIO
53	+VCCSA
54	+5V_DUAL
55	+12V_+5V_AUX/+1V_PCH
56	+1P35V_DUAL
57	+VTT_DDR
58	+5V_AUX/+3P3V_SB
59	+3P3V_AUX
60	POWER -12V
61	EUP
62	CHANGELIST

Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

Project Information

Phase: SMVB

Ver: X4

SVID: 103C

SSID: 2B5E

Form factor:uATX

BOM DISTRIBUTION RULE


Manny , Sid
(BOM,BOM)

Project	Description	PCA PN	SCH PN (DG#)	PCB PN	ASSY CODE
Iceage	MCP,Manny,Intel,Iceage,H110,MT	828984-001	828985-000	828986-001	PHTA
	MAD,Sid,Intel,Iceage,H110,MT	828984-002	828985-000	828986-001	PHTB

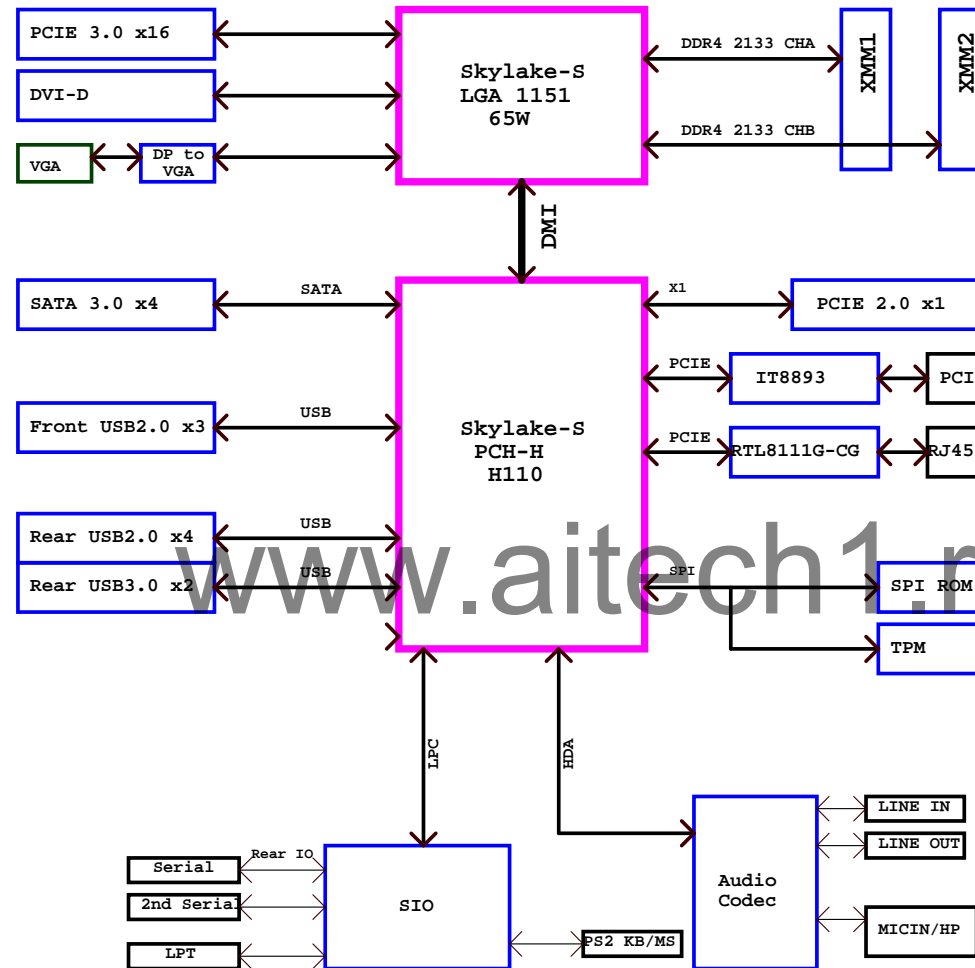
Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
EVT	RED	YELLOW
DVT	LIGHT BLUE	YELLOW
PVT/MVB / PRODUCTION	GREEN	WHITE


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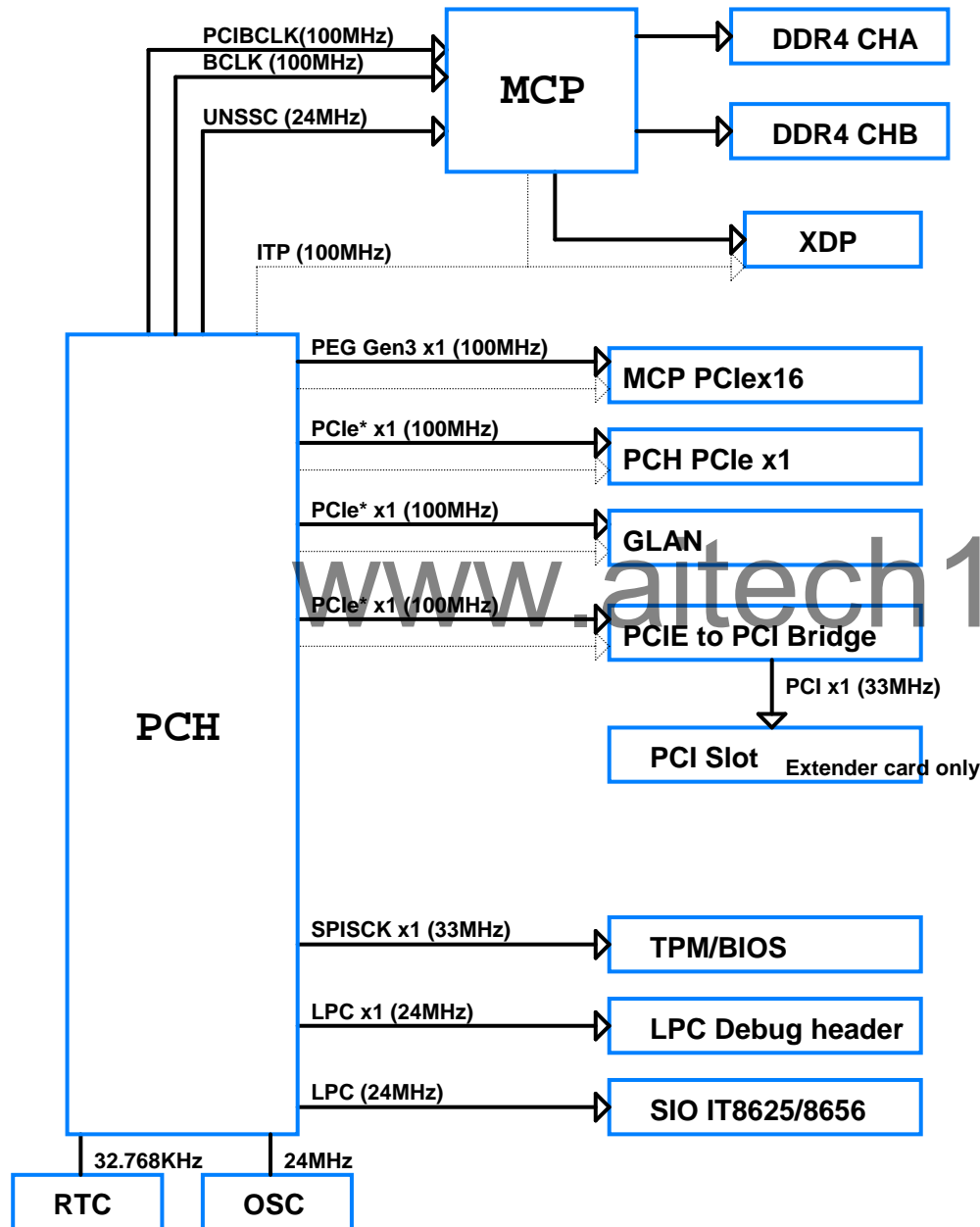
System BLOCK Diagram




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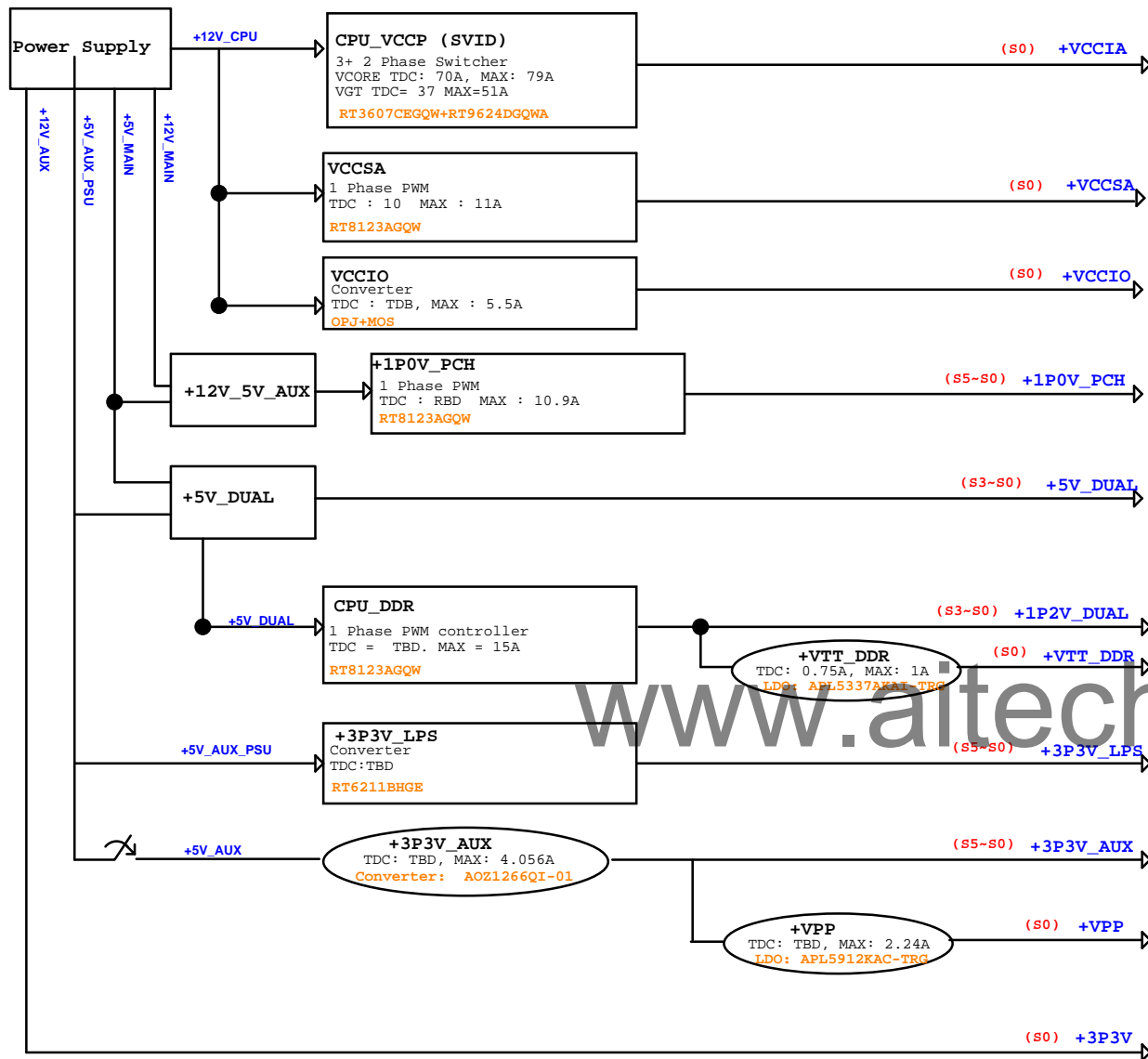
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Clock Diagram



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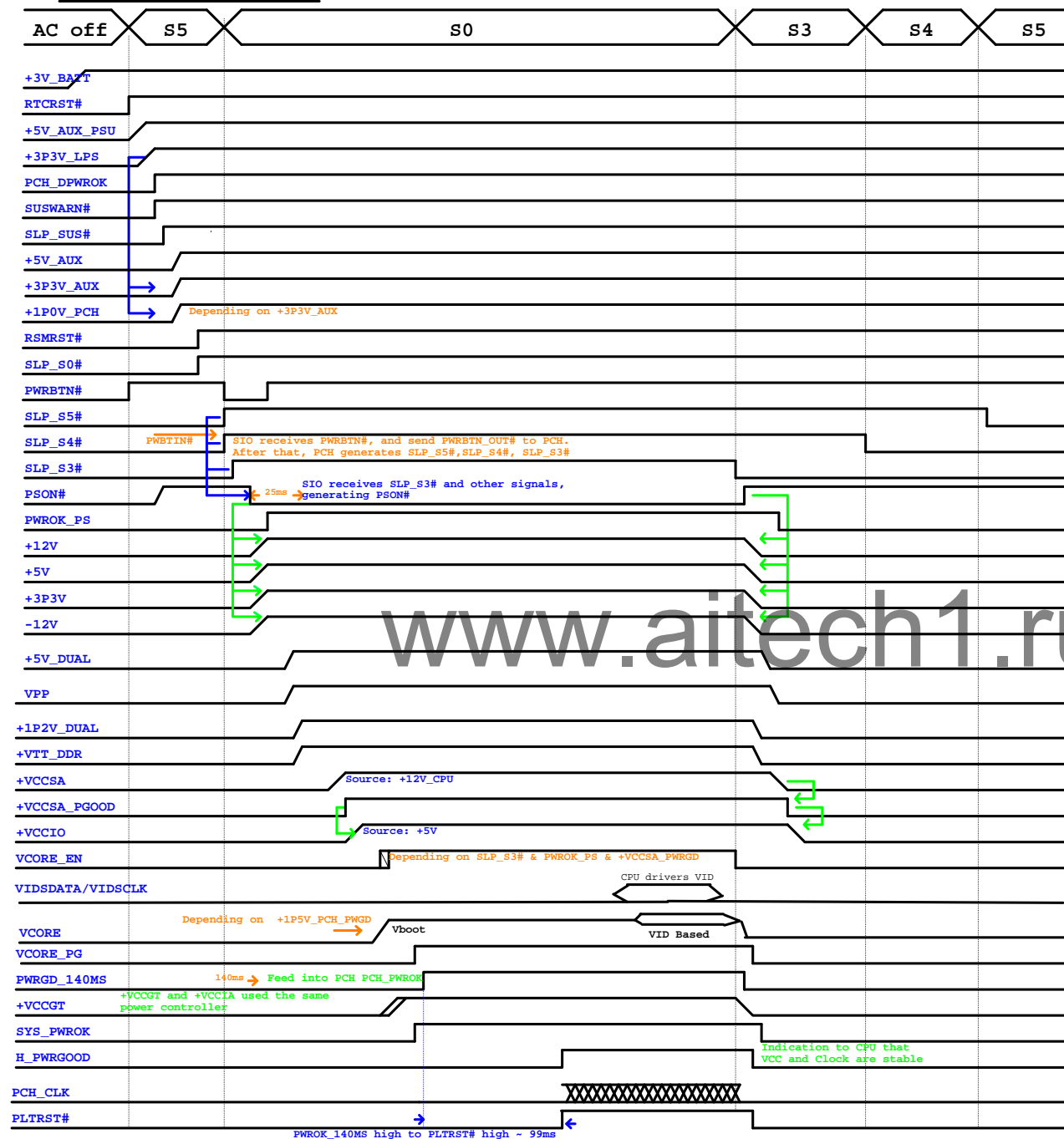
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Date: Tuesday, November 17, 2015	Sheet: 5	of: 62	

[illegible]

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[illegible]

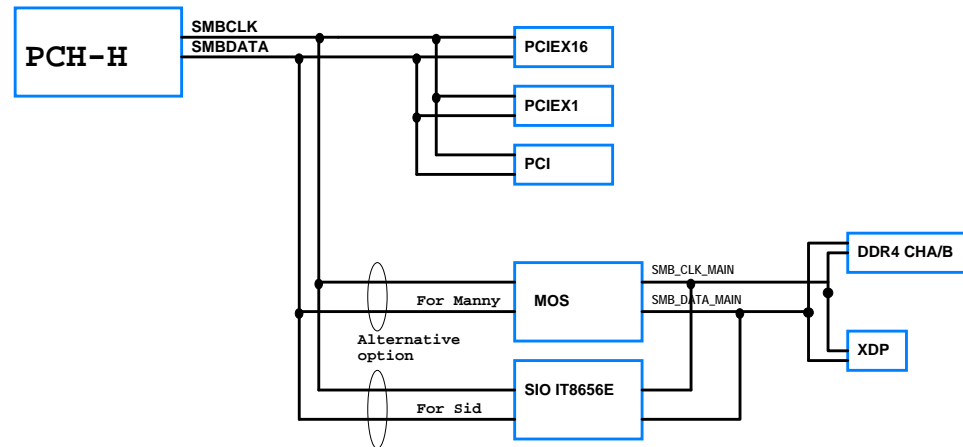
POWER SEQUENCE DIAGRAM



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SM Bus MAP



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Title INTERRUPT & PME DIAGRAM					
Size	Document Number				Rev
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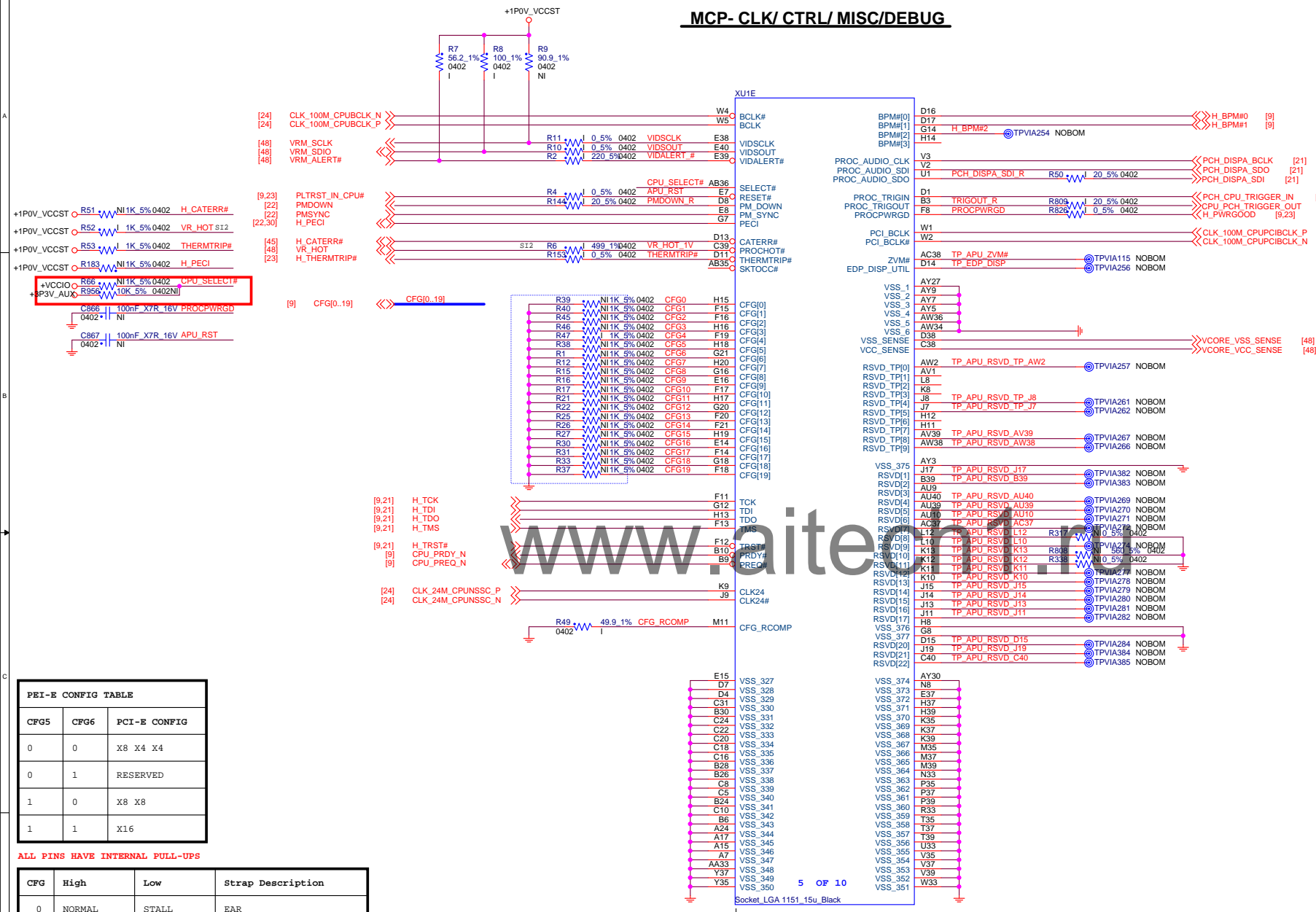
The diagram illustrates the Intel MCP XDP Debug Connector, showing various signal connections, component values, and component footprints. The components are organized into several sections:

- Top Section:** Includes components like R87, R88, R86, R792, and R791, connected to +1P0V_PCH, +3P3V_AUX +VCCIO, and +1P0V_PCH.
- Left Section:** Lists various signals and their connections, including SIO_RSMRST#, H_PWRGOOD, VCORE_PG_BF, PWRBTN_OUT#, SYS_PWROK, SPI_MOSI, CLK_100M_I/P_P, CLK_100M_I/P_N, PCH_I/P_PMODE, PLTRST_IN_CPU#, FP_RST#, H_TCK, PCH_JTAG_TCK_R, H_TDI, H_TDO, H_TMS, H_TRST#, SMB_DATA_MAIN, and SMB_CLK_MAIN.
- Right Section:** Lists various signals and their connections, including XDP_RSMRST#, XDP_PWRBTN_OUT#, XDP_HOOK2, XDP_HOOK3, XDP_CLK_100M_H_I/P#, XDP_I/P_PMODE, XDP_FP_RST#, H_TCK, H_TCK1, H_TDO, H_TMS, H_TRST#, XDP_PRESENT#_CPU, XDP_PRESENT#_R, XDP_CPU_OBSFN_B0, XDP_CPU_OBSFN_B1, XDP_CPU_DATA_B0, XDP_CPU_DATA_B1, XDP_CPU_DATA_B2, XDP_CPU_DATA_B3, XDP_CPU_OBSFN_C0, XDP_CPU_OBSFN_C1, XDP_CPU_DATA_C1, XDP_CPU_DATA_C2, XDP_CPU_DATA_C3, XDP_CPU_OBSFN_D0, XDP_CPU_OBSFN_D1, XDP_CPU_DATA_D0, XDP_CPU_DATA_D1, XDP_CPU_DATA_D2, XDP_CPU_DATA_D3, VCC_OBS_AB, VCC_OBS_CD, NP_NC_1, NP_NC_2, and ITP_2X30_GF.
- Bottom Section:** Includes components like R89, R79, R79, R92, R793, R791, R93, R94, R95, R96, R790, R150, R890, R59, R100, R97, R892, C75, C74, R102, R825, and R825, connected to various signals and ground.

The diagram also includes a note about VCCST Power Gating (Q1) implemented: XDP_PRESENT# need connect to Q1.G with a inverse logic.

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MCP- CLK/ CTRL/ MISC/DEBUG




PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

ALL PINS HAVE INTERNAL PULL-UPS

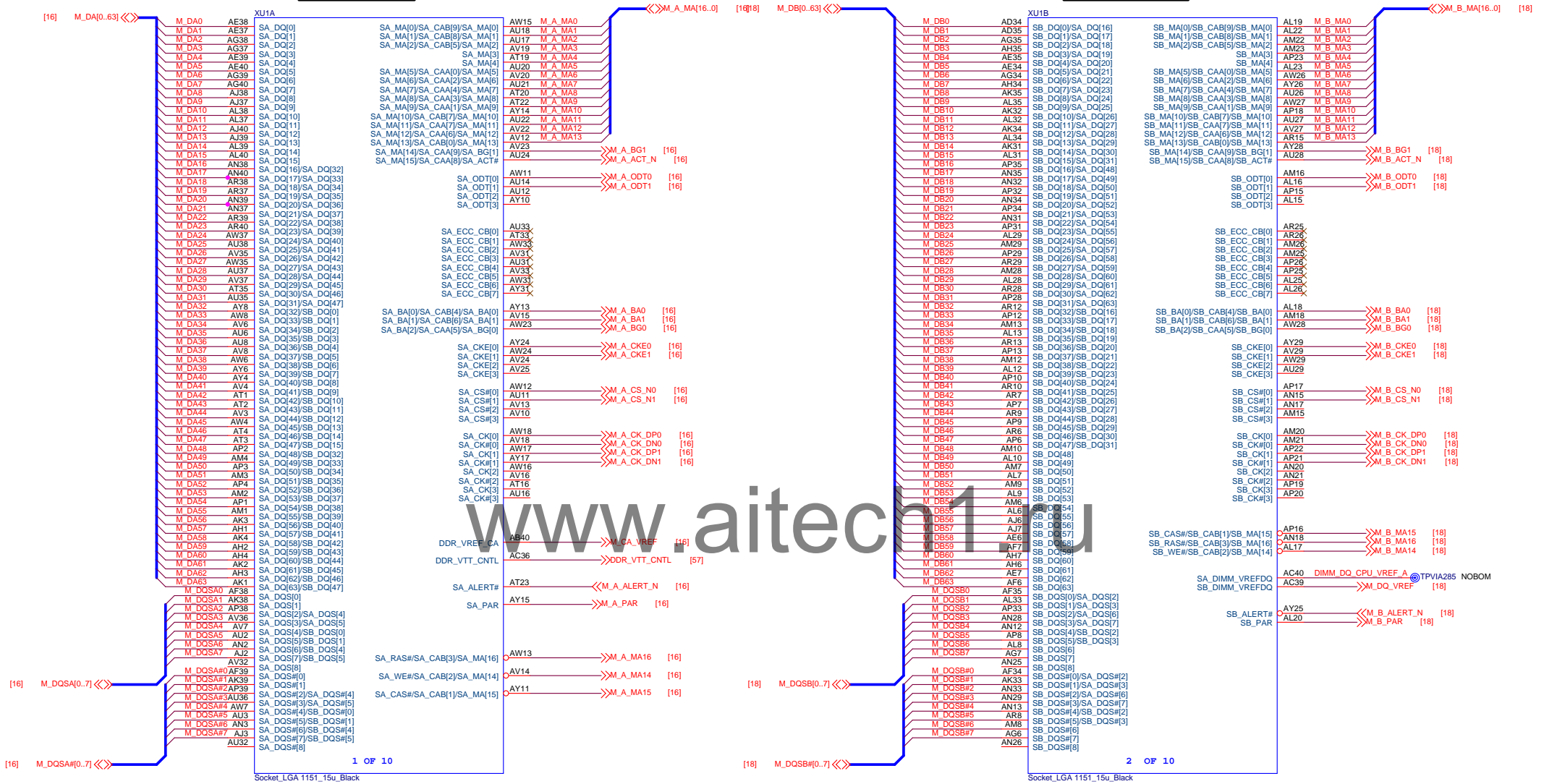
CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1			RESERVED
2	NORMAL	REVERSE	PEG LANE REVERSAL
3			RESERVED
4	DISABLE see table above	ENABLE "0"	eDP enable
5	see table above		PEG0CFGSEL[0] x16
6	see table above		PEG0CFGSEL[1] x16
7	RESET N	BIOS REQ	PEG DEFER TRAINING
8-19			RESERVED

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Size Customer	Document Number 828985-000		Rev 0.1
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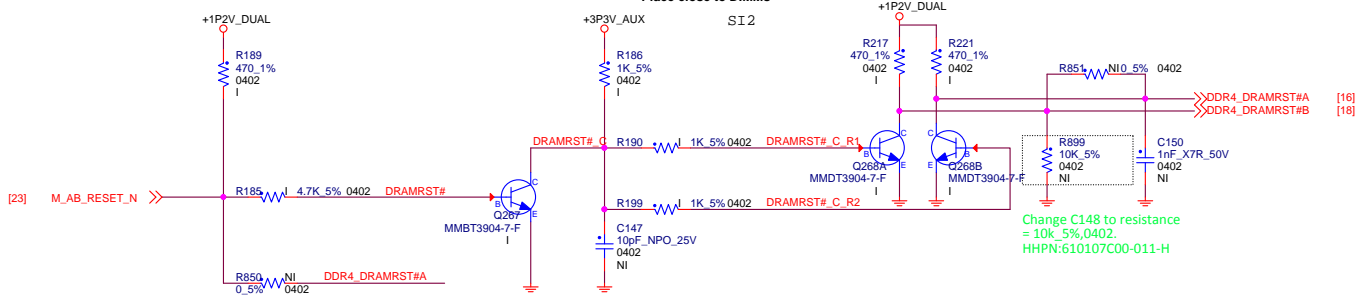
DDR4 CH-A

DDR4 CH-B



DDR4 DRAMRST# BUFFER CIRCUIT

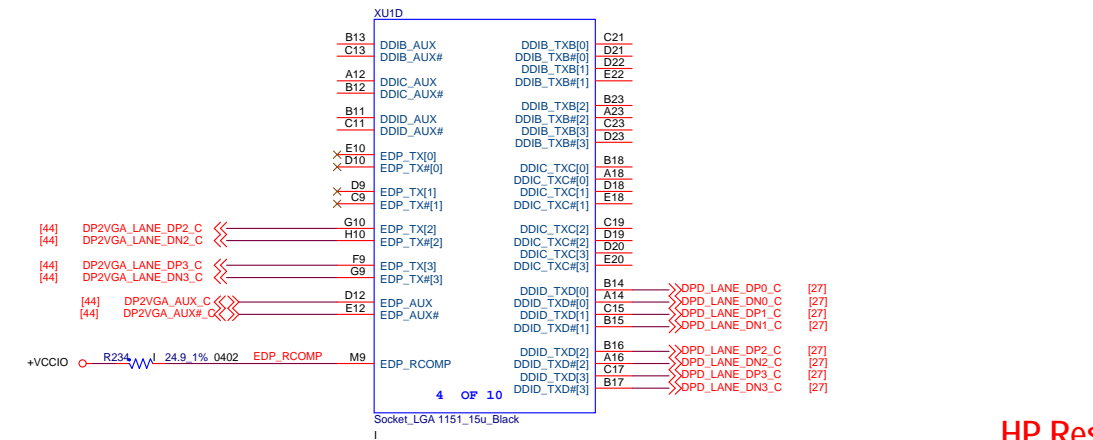
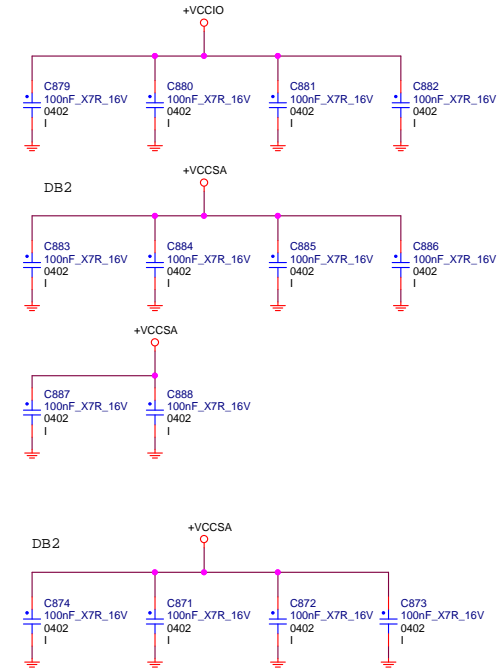
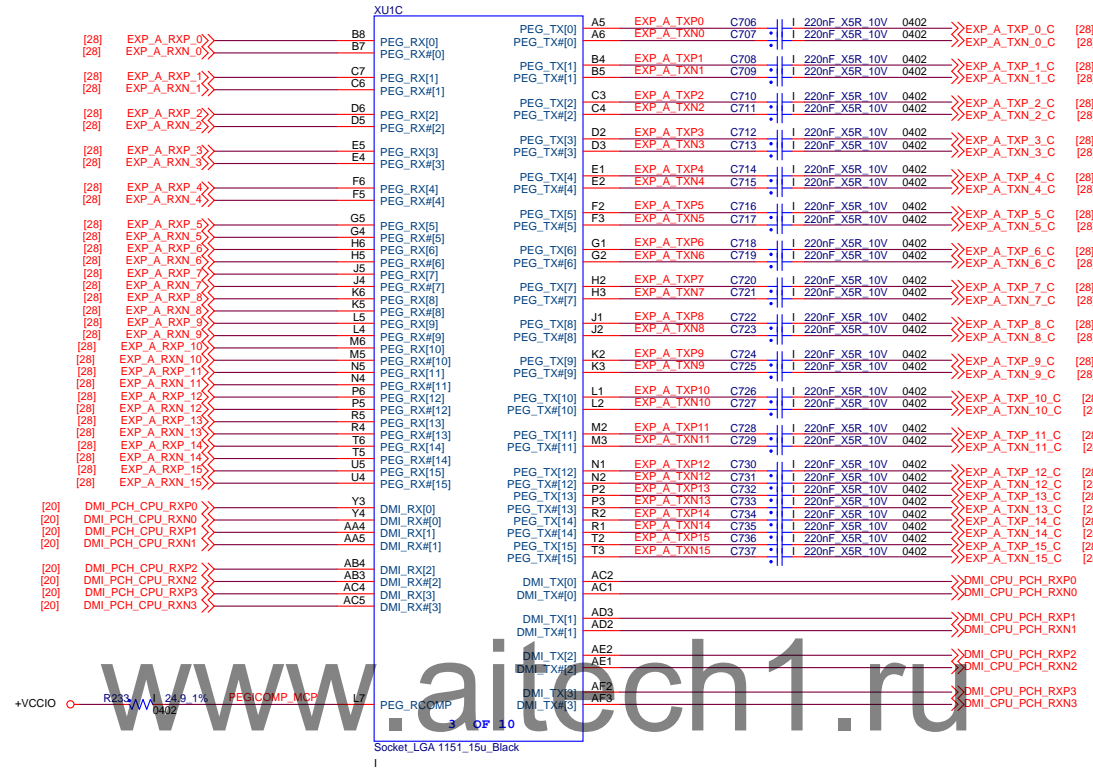
Place close to DIMMs



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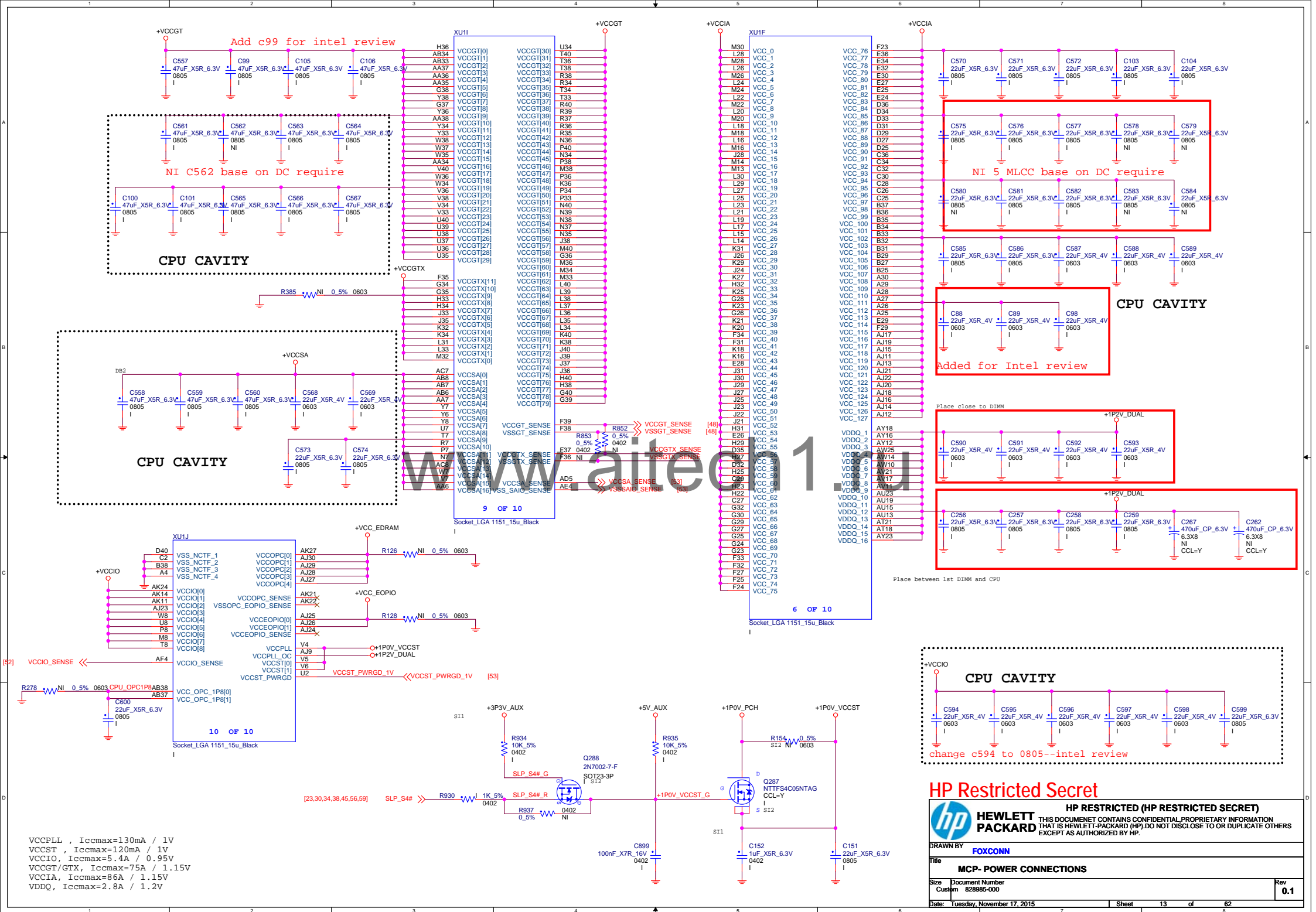
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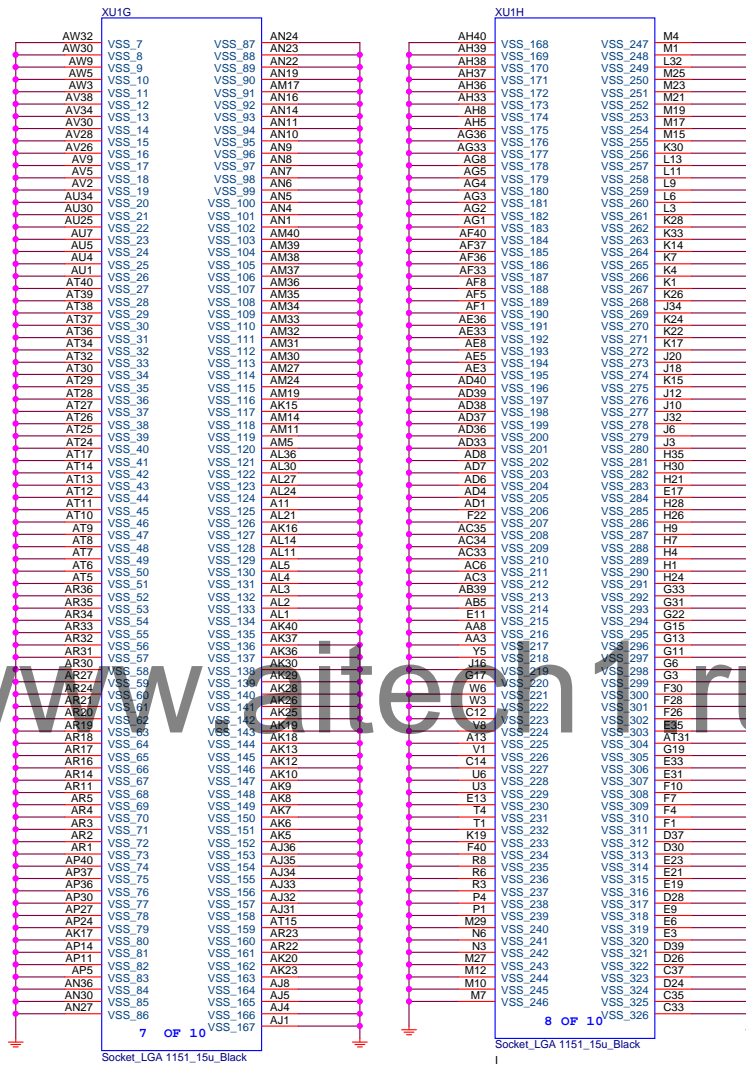
MCP - PCIE,DMI,FDI,DDI




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Size	Document Number	Rev			
Custom	828985-000	0.1			
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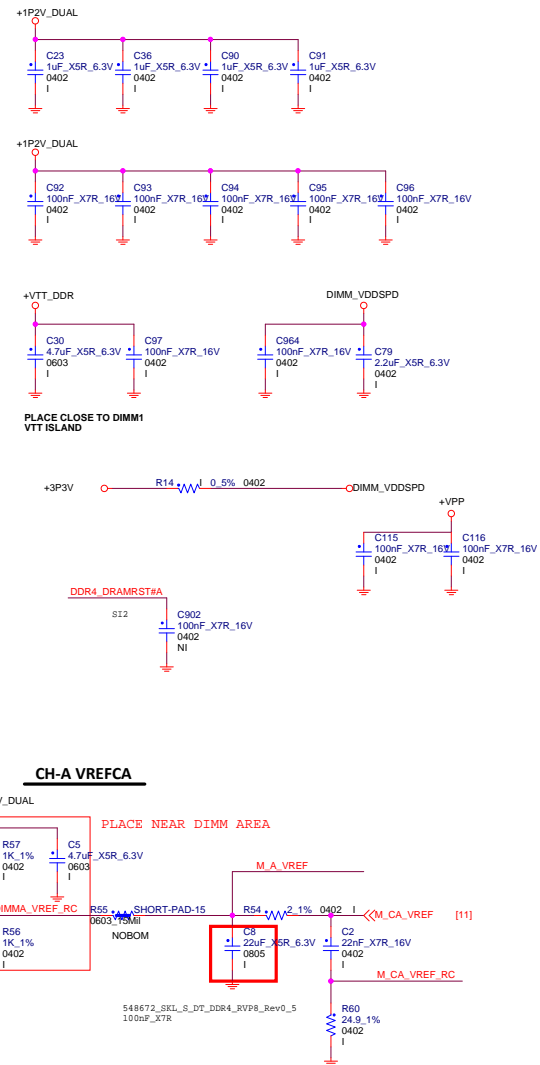
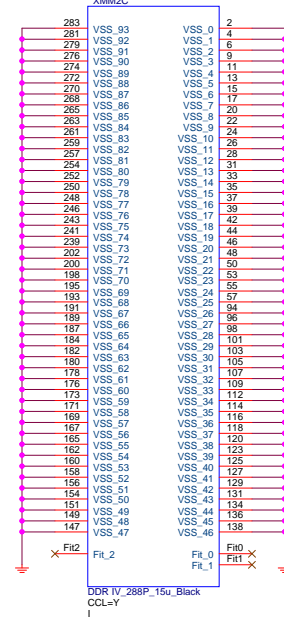
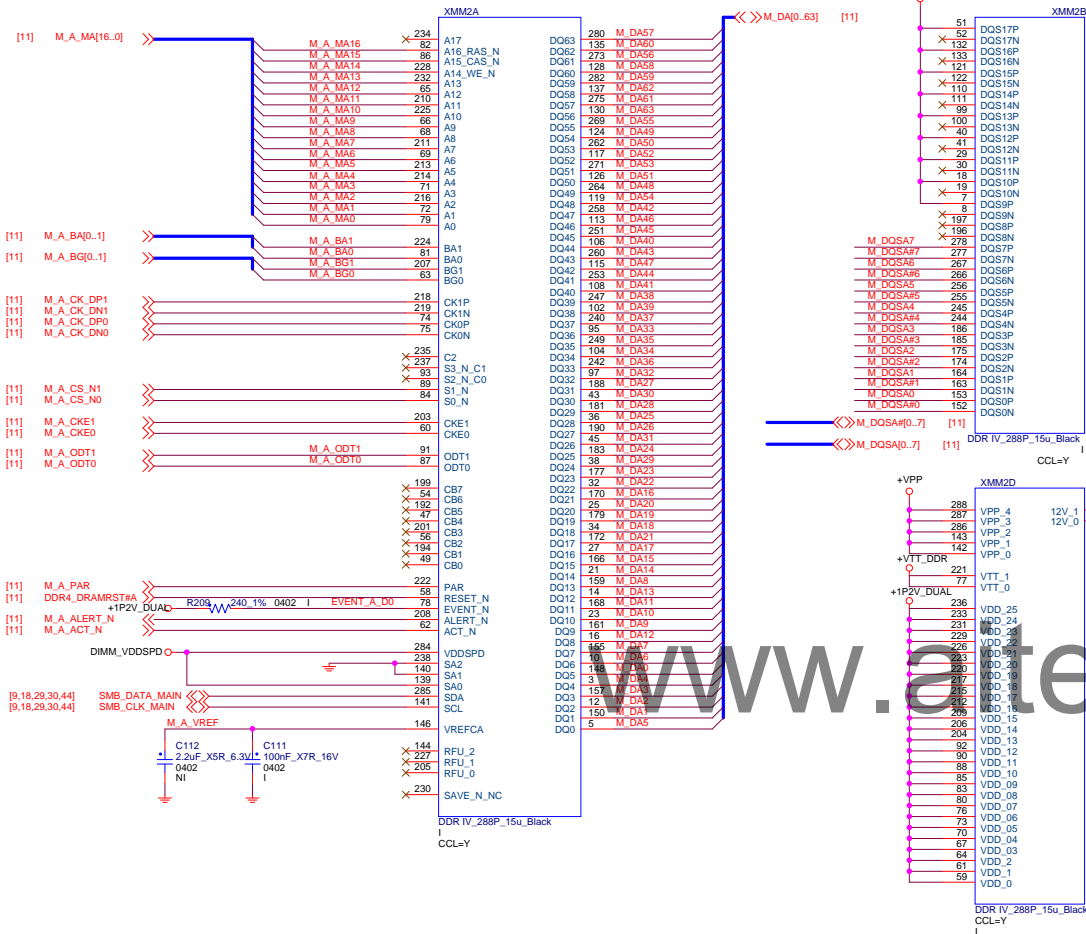
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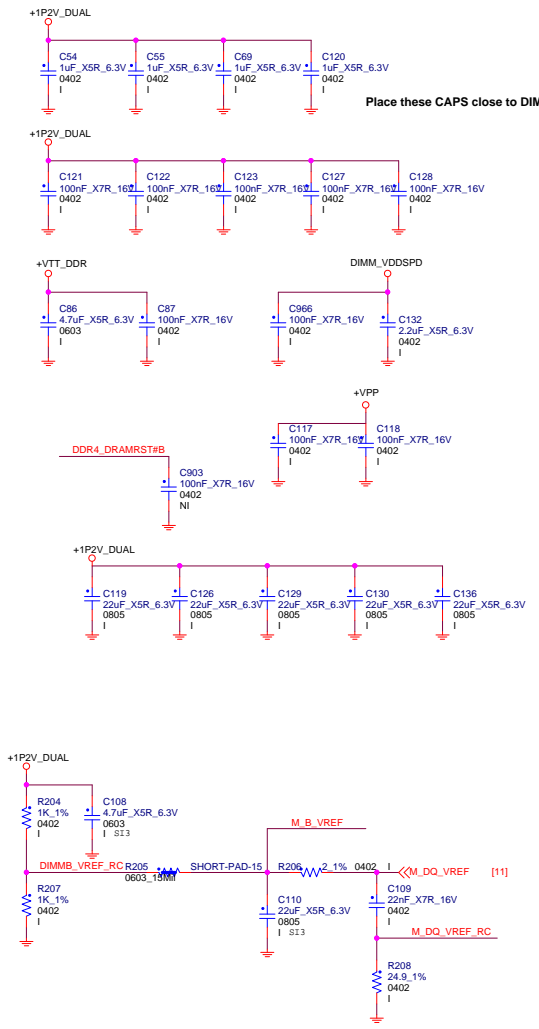
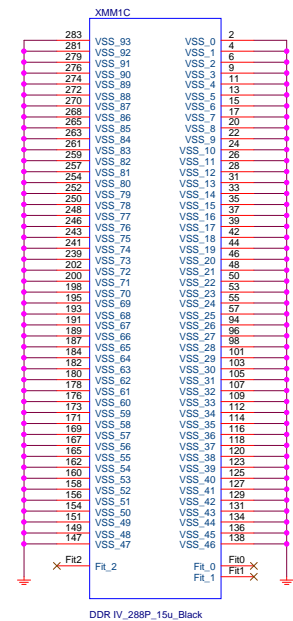
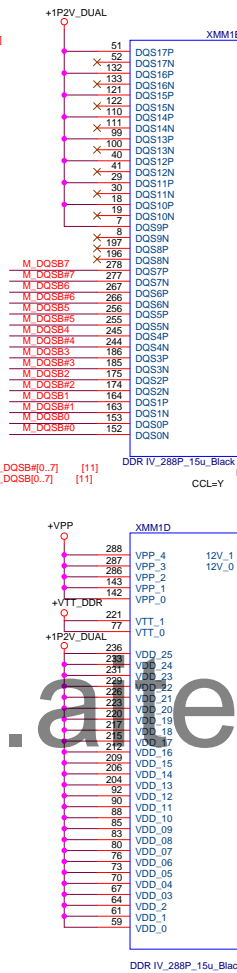
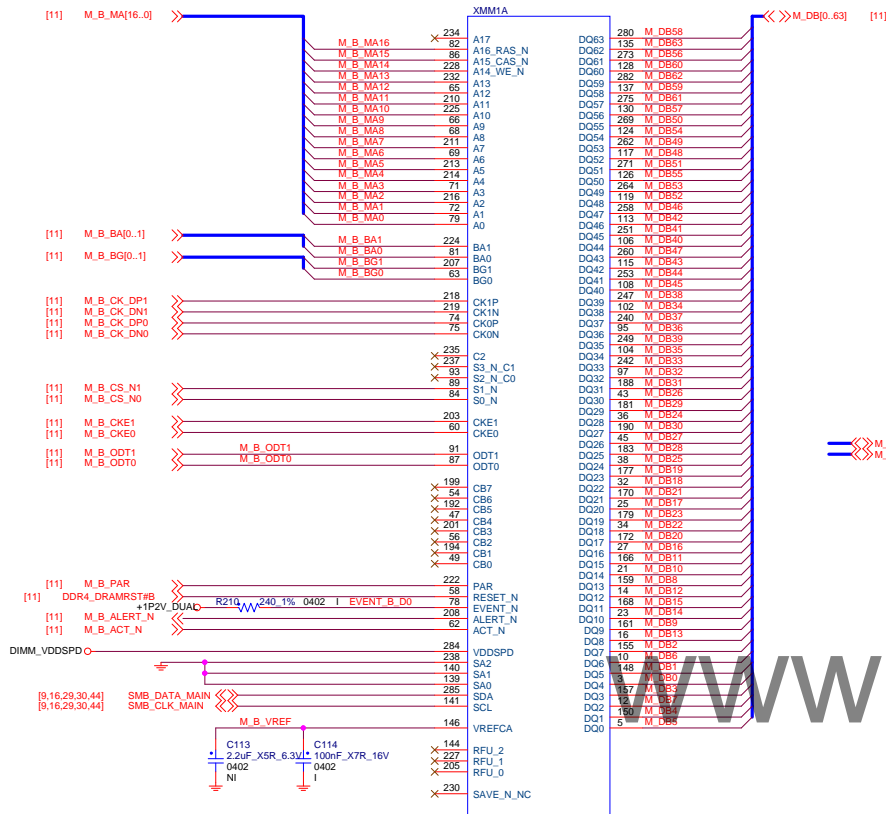
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Title DDR4 CHA D0 XMM2			
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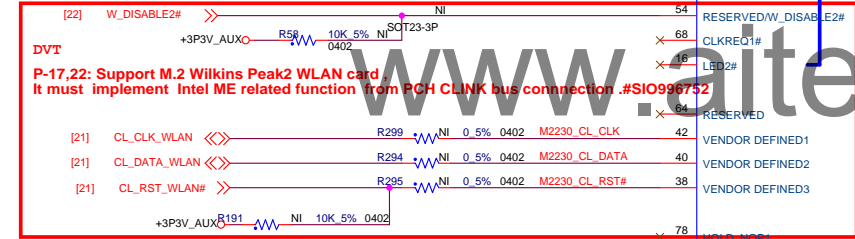
HP is discussing about swap DDR SPD address, will determine before PV phase, reserve the short pad for rework probability. will remove short pad at that time.
SPD ADDRESS: 000
SMBUS ADDRESS: A0

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Title DDR4 CHB D0 XMM1			
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J86
FOXCONN_AS0BC26-S40BA-7H
CCL=Y
NI

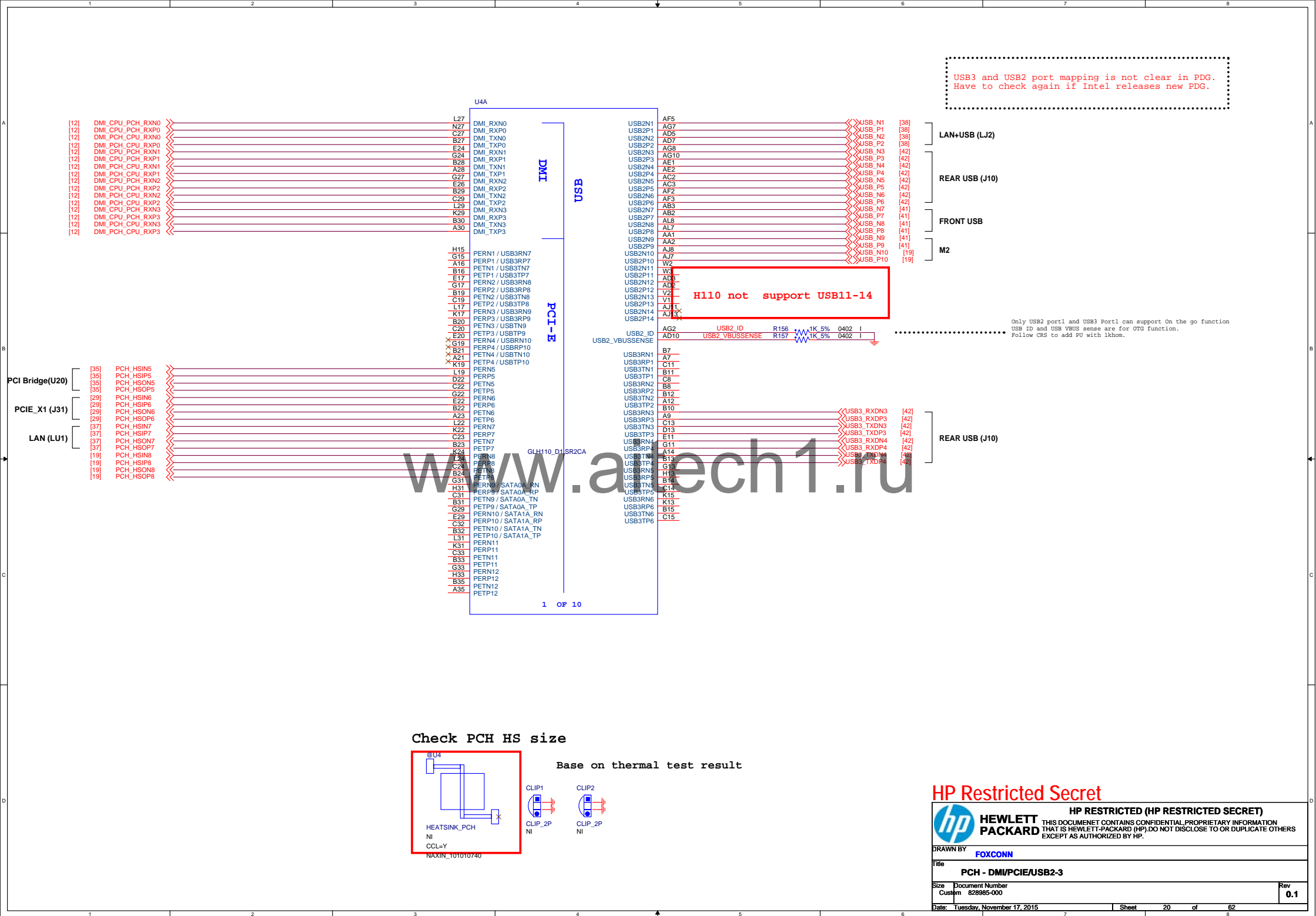
+3P3V_AUX

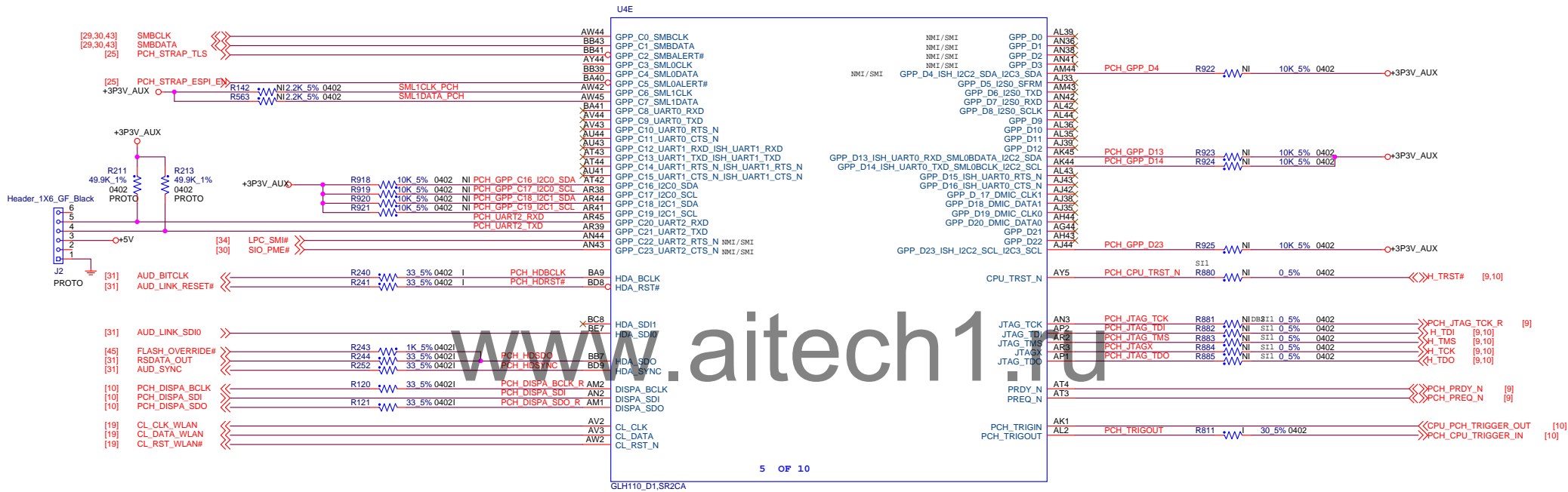


NUT2
EMI_F55M30-250740P1D4AM
CCL=Y
NI




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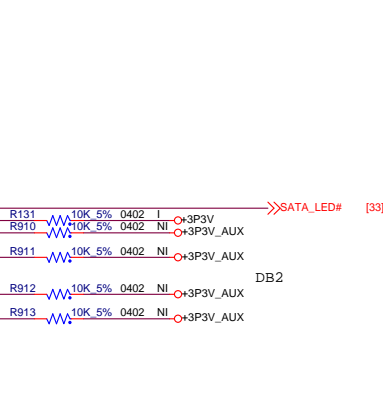
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[39] SATA_RXP0
[39] SATA_TXN0
[39] SATA_TXP0
[39] SATA_RXN1
[39] SATA_RXP1
[39] SATA_TXN1
[39] SATA_TXP1
[39] SATA_RXN2
[39] SATA_RXP2
[39] SATA_TXN2
[39] SATA_TXP2
[39] SATA_RXN3
[39] SATA_RXP3
[39] SATA_TXN3
[39] SATA_TXP3



G35 SATA_RXN0B / PERN13
E35 SATA_RXP0B / PERP13
C36 SATA_TXN0B / PETN13
B36 SATA_TXP0B / PETP13
D39 SATA_RXN1B / PERN14
E37 SATA_RXP1B / PERP14
B38 SATA_TXN1B / PETN14
C38 SATA_TXP1B / PETP14
F41 SATA_RXN2 / PERN15
E41 SATA_RXP2 / PERP15
B39 SATA_TXN2 / PETN15
A39 SATA_TXP2 / PETP15
D43 SATA_RXN3 / PERN16
E42 SATA_RXP3 / PERP16
A41 SATA_TXN3 / PETN16
A40 SATA_TXP3 / PETP16
H42 SATA_RXN4 / PERN17
H40 SATA_RXP4 / PERP17
F45 SATA_TXN4 / PETN17
K37 SATA_TXP4 / PETP17
G37 SATA_RXN5 / PERN18
G45 SATA_RXP5 / PERP18
L37 SATA_TXN5 / PETN18
L39 SATA_TXP5 / PERP18
H43 SATA_RXN6 / PERN19
H44 SATA_RXP6 / PERP19
N38 SATA_TXN6 / PETN19
N39 SATA_TXP6 / PETP19
K44 SATA_RXN7 / PERN20
J45 SATA_RXP7 / PERP20
SATA_TXP7 / PETN20

GPP_E0_SATAXPIC0_SATAGP0
GPP_E1_SATAXPIC1_SATAGP1
GPP_E2_SATAXPIC2_SATAGP2
GPP_F0_SATAXPIC3_SATAGP3
GPP_F1_SATAXPIC4_SATAGP4
GPP_F2_SATAXPIC5_SATAGP5
GPP_F3_SATAXPIC6_SATAGP6
GPP_F4_SATAXPIC7_SATAGP7
GPP_E8_SATALED_N
GPP_F10_SCLK
GPP_F11_SLOAD
GPP_F12_SDATOUT1
GPP_F13_SDATOUT0
GPP_F19_EDP_VDDEN
GPP_F20_EDP_BKLTEN
GPP_F21_EDP_BKLTCTL
GPP_E3_CPU_GP0
GPP_E7_CPU_GP1
GPP_E4_DEVSLP0
GPP_E5_DEVSLP1
GPP_E6_DEVSLP2
GPP_F5_DEVSLP3
GPP_F6_DEVSLP4
GPP_F7_DEVSLP5
GPP_F8_DEVSLP6
GPP_F9_DEVSLP7
GPP_I0_DDPB_HP00
GPP_I1_DDPB_HP01
GPP_I2_DDPB_HP02
GPP_I3_DDPB_HP03
GPP_I4_EDP_HP0
GPP_I5_DDPB_CTRLCLK
GPP_I6_DDPB_CTRLCLK
GPP_I7_DDPB_CTRLCLK
GPP_I8_DDPB_CTRLCLK
GPP_I9_DDPB_CTRLCLK
GPP_I10_DDPB_CTRLCLK

AG36
AG35
AG39
AD35
AD31
AD38
AC43
AB44
AD44
AB33 PCH_GPP_F10_SCLK
AB35 PCH_GPP_F11_SLOAD
AA45 PCH_GPP_F12_SDATOUT1
AA44 PCH_GPP_F13_SDATOUT0
W42
W35
W36
Y44
W39
V44
AD43
AD42
AD39
AC44
Y43
Y41 PCH_GPP_F16_USB2_OC3_N
W44 PCH_GPP_F17_USB2_OC4_N
W43 PCH_GPP_F18_USB2_OC7_N
AD43
AD42
AD39
AC44
Y43
Y41
W44
W43



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

[27] DDPD_HP0_R
[44] DPE_HP0_R



AW4
AY2
AV4
BA4
BD7
BA5
BC4
BB3
BD6
BE5
BE6

GPP_I0_DDPB_HP00
GPP_I1_DDPB_HP01
GPP_I2_DDPB_HP02
GPP_I3_DDPB_HP03
GPP_I4_EDP_HP0
GPP_I5_DDPB_CTRLCLK
GPP_I6_DDPB_CTRLCLK
GPP_I7_DDPB_CTRLCLK
GPP_I8_DDPB_CTRLCLK
GPP_I9_DDPB_CTRLCLK
GPP_I10_DDPB_CTRLCLK

GPP_E9_USB2_OC0_N
GPP_E10_USB2_OC1_N
GPP_E11_USB2_OC2_N
GPP_E12_USB2_OC3_N
GPP_F15_USB2_OC4_N
GPP_F16_USB2_OC5_N
GPP_F17_USB2_OC6_N
GPP_F18_USB2_OC7_N



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

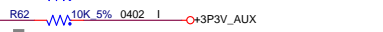
[27] DDPD_CTRLCLK
[27] DDPD_CTRLCLK



AW4
AY2
AV4
BA4
BD7
BA5
BC4
BB3
BD6
BE5
BE6

GPP_I0_DDPB_HP00
GPP_I1_DDPB_HP01
GPP_I2_DDPB_HP02
GPP_I3_DDPB_HP03
GPP_I4_EDP_HP0
GPP_I5_DDPB_CTRLCLK
GPP_I6_DDPB_CTRLCLK
GPP_I7_DDPB_CTRLCLK
GPP_I8_DDPB_CTRLCLK
GPP_I9_DDPB_CTRLCLK
GPP_I10_DDPB_CTRLCLK

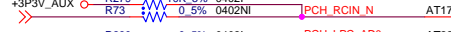
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GPP_E10_USB2_OC1_N
GPP_E11_USB2_OC2_N
GPP_E12_USB2_OC3_N
GPP_F15_USB2_OC4_N
GPP_F16_USB2_OC5_N
GPP_F17_USB2_OC6_N
GPP_F18_USB2_OC7_N



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

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[30] SIO_KBRST#



AT17
AT22
AT19
BD16
BE16
BA17
AW17
AW22
BC17
AV19
BD17
BD19
BC18
BB19
AR17
BC19
BB22
BD21
BD22
BE21
BD18
BC22

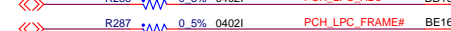
GPP_A0_RCIN_N_ESPI_ALERT1_N
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GPP_A2_LAD1_ESPI_I01
GPP_A3_LAD2_ESPI_I02
GPP_A4_LAD3_ESPI_I03
GPP_A5_LFRAME_N_ESPI_CS0_N
GPP_A6_SERIRQ_ESPI_CS1_N
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_A11_PME_N
GPP_A12_BMBUSY_N_ISH_GP6_SX_EXIT_HOLD0FF_N
GPP_A13_SUSWARN_N_SUSWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RESET_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5

GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

[30,34] LPC_AD0
[30,34] LPC_AD1
[30,34] LPC_AD2
[30,34] LPC_AD3



AT17
AT22
AT19
BD16
BE16
BA17
AW17
AW22
BC17
AV19
BD17
BD19
BC18
BB19
AR17
BC19
BB22
BD21
BD22
BE21
BD18
BC22

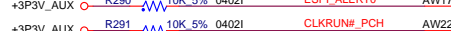
GPP_A0_RCIN_N_ESPI_ALERT1_N
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GPP_A3_LAD2_ESPI_I02
GPP_A4_LAD3_ESPI_I03
GPP_A5_LFRAME_N_ESPI_CS0_N
GPP_A6_SERIRQ_ESPI_CS1_N
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_A11_PME_N
GPP_A12_BMBUSY_N_ISH_GP6_SX_EXIT_HOLD0FF_N
GPP_A13_SUSWARN_N_SUSWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RESET_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5

GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

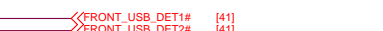
[30] CK_P_24M_SIO
[30] CK_24M_SIO
[34] LPC_DEBUG_CLK
[30] SIO2PCH_SMI#



AT17
AT22
AT19
BD16
BE16
BA17
AW17
AW22
BC17
AV19
BD17
BD19
BC18
BB19
AR17
BC19
BB22
BD21
BD22
BE21
BD18
BC22

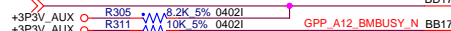
GPP_A0_RCIN_N_ESPI_ALERT1_N
GPP_A1_LAD0_ESPI_I00
GPP_A2_LAD1_ESPI_I01
GPP_A3_LAD2_ESPI_I02
GPP_A4_LAD3_ESPI_I03
GPP_A5_LFRAME_N_ESPI_CS0_N
GPP_A6_SERIRQ_ESPI_CS1_N
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_A11_PME_N
GPP_A12_BMBUSY_N_ISH_GP6_SX_EXIT_HOLD0FF_N
GPP_A13_SUSWARN_N_SUSWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RESET_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5

GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

[30] SUS_WARN#



AT17
AT22
AT19
BD16
BE16
BA17
AW17
AW22
BC17
AV19
BD17
BD19
BC18
BB19
AR17
BC19
BB22
BD21
BD22
BE21
BD18
BC22

GPP_A0_RCIN_N_ESPI_ALERT1_N
GPP_A1_LAD0_ESPI_I00
GPP_A2_LAD1_ESPI_I01
GPP_A3_LAD2_ESPI_I02
GPP_A4_LAD3_ESPI_I03
GPP_A5_LFRAME_N_ESPI_CS0_N
GPP_A6_SERIRQ_ESPI_CS1_N
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_A11_PME_N
GPP_A12_BMBUSY_N_ISH_GP6_SX_EXIT_HOLD0FF_N
GPP_A13_SUSWARN_N_SUSWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RESET_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5

GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

[30] SUS_PWR_ACK#



AT17
AT22
AT19
BD16
BE16
BA17
AW17
AW22
BC17
AV19
BD17
BD19
BC18
BB19
AR17
BC19
BB22
BD21
BD22
BE21
BD18
BC22

GPP_A0_RCIN_N_ESPI_ALERT1_N
GPP_A1_LAD0_ESPI_I00
GPP_A2_LAD1_ESPI_I01
GPP_A3_LAD2_ESPI_I02
GPP_A4_LAD3_ESPI_I03
GPP_A5_LFRAME_N_ESPI_CS0_N
GPP_A6_SERIRQ_ESPI_CS1_N
GPP_A7_PIRQA_N_ESPI_ALERT0_N
GPP_A8_CLKRUN_N
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_A11_PME_N
GPP_A12_BMBUSY_N_ISH_GP6_SX_EXIT_HOLD0FF_N
GPP_A13_SUSWARN_N_SUSWRDNACK
GPP_A14_SUS_STAT_N_ESPI_RESET_N
GPP_A15_SUSACK_N
GPP_A16_CLKOUT_48
GPP_A17_ISH_GP7
GPP_A18_ISH_GP0
GPP_A19_ISH_GP1
GPP_A20_ISH_GP2
GPP_A21_ISH_GP3
GPP_A22_ISH_GP4
GPP_A23_ISH_GP5

GPP_G0_FAN_TACH_0
GPP_G1_FAN_TACH_1
GPP_G2_FAN_TACH_2
GPP_G3_FAN_TACH_3
GPP_G4_FAN_TACH_4
GPP_G5_FAN_TACH_5
GPP_G6_FAN_TACH_6
GPP_G7_FAN_TACH_7
GPP_G8_FAN_PWM_0
GPP_G9_FAN_PWM_1
GPP_G10_FAN_PWM_2
GPP_G11_FAN_PWM_3
GPP_G12_GSXDOUT
GPP_G13_GSXSLOAD
GPP_G14_GSXDIN
GPP_G15_GSXSRESET_N
GPP_G16_GSXCCLK
GPP_G17_ADR_COMPLETE
GPP_G18_NMI_N
GPP_G19_SMI_N
GPP_G20
GPP_G21
GPP_G22
GPP_G23



Need to check Intel design guide for OC# port mapping
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]

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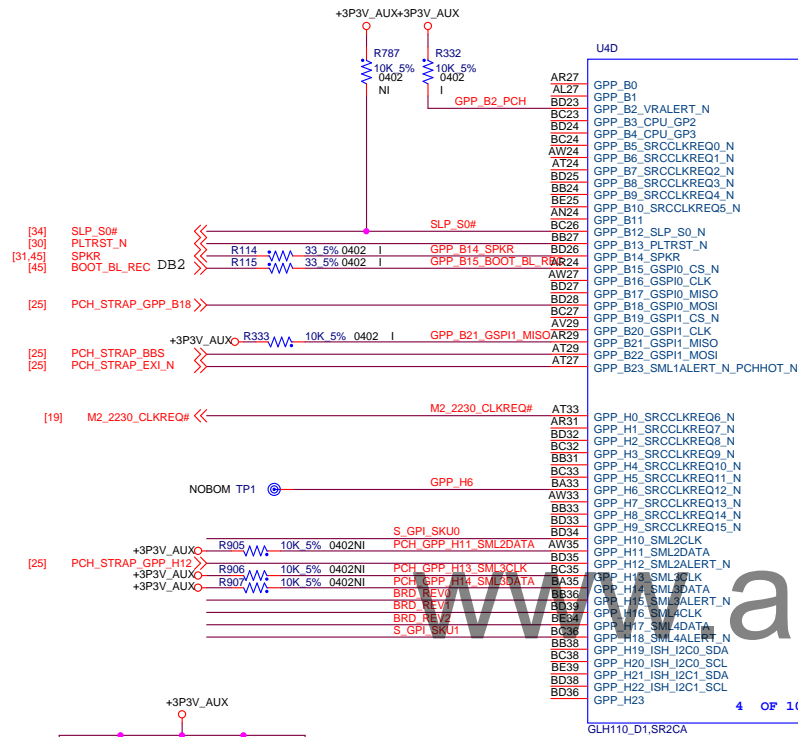
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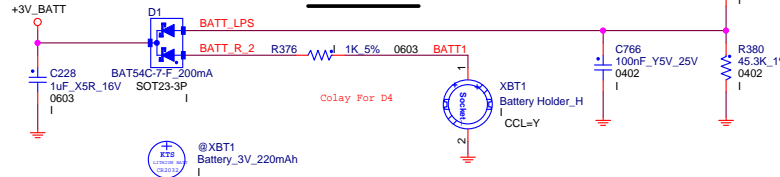
Title **PCH - SATA/SPI/GPIO**

Size Document Number **828985-000** Rev **0.1**

Date: **Tuesday, November 17, 2015** Sheet **22** of **62**



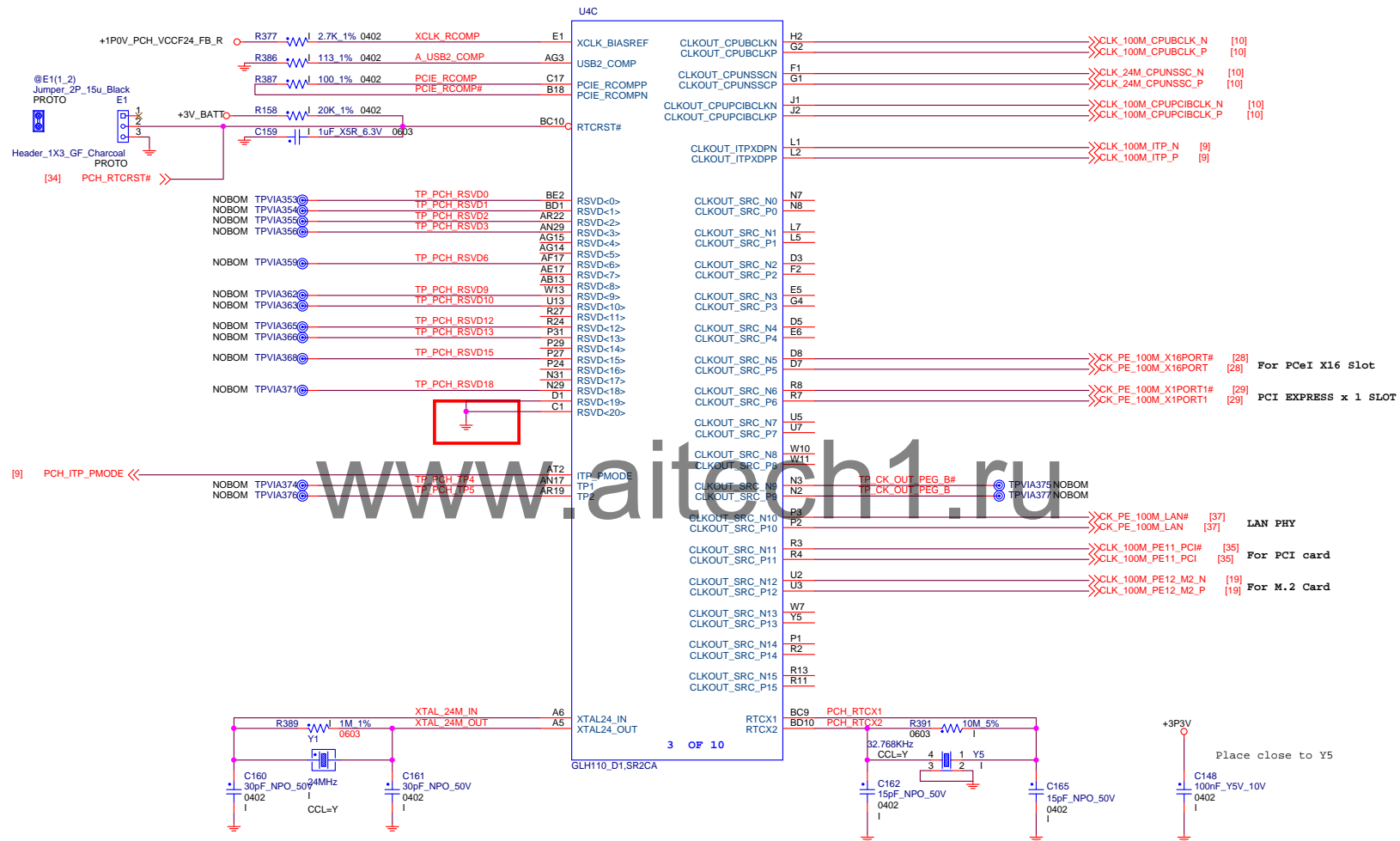
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HEWLETT PACKARD		THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP) DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.	
DRAWN BY FOXCONN			
Title PCH - GPIO/MISC			
Size	Document Number	Rev	
Custom	828965-000	0.1	
Date:	Tuesday, November 17, 2015	Sheet	23 of 62

PCH - CLOCK DISTRIBUTION

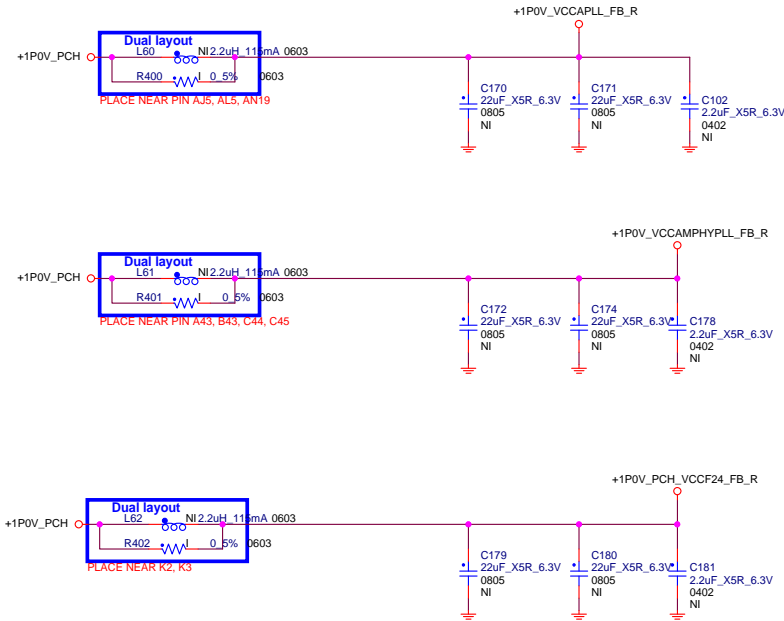


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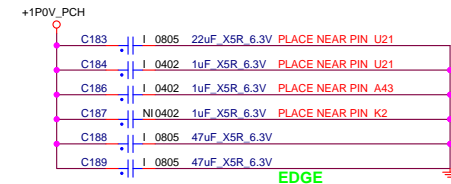
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		<small>THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP) DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.</small>			
DRAWN BY FOXCONN					
Title PCH - CLOCK					
Size	Document Number	Rev			
Custom	828985-000	0.1			
Date: Tuesday, November 17, 2015		Sheet		24	of 62

SKYLAKE Decoupling & filter

FILTER



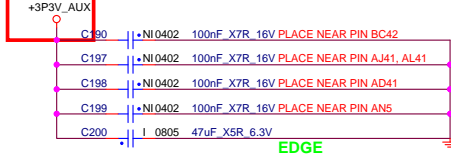
V1.0A



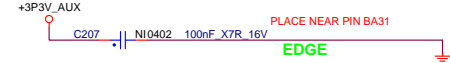
V3.3 DSW



V1.8A / V3.3A



VccPGPPA



V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC




Power Plane Isolation

Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

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Title **PCH-PLL FILTER & DECOUPLING**

Size Document Number
Custom 828965-000

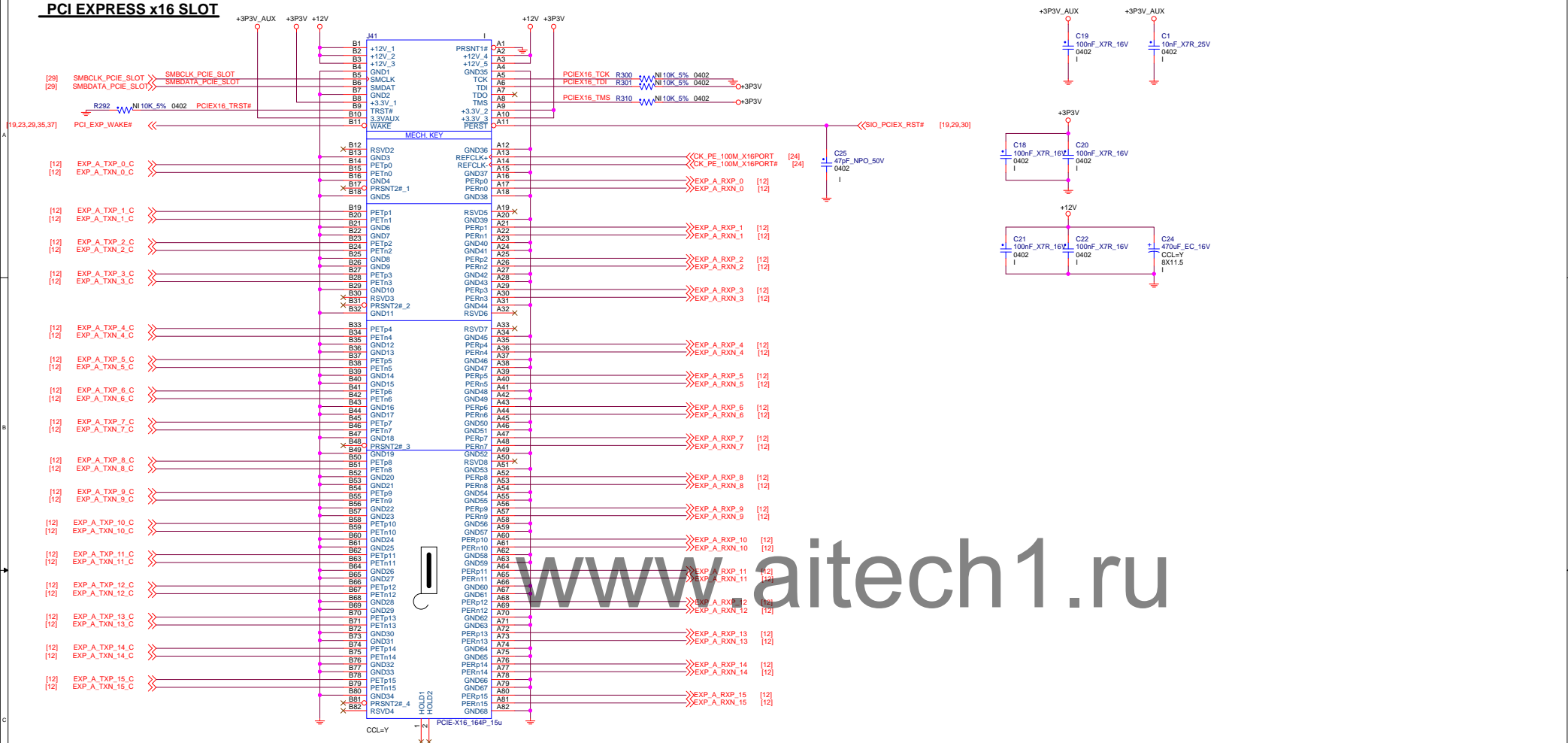
Date: Tuesday, November 17, 2015

Sheet 26 of 62

Rev **0.1**

0.1

PCI EXPRESS x16 SLOT



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Title

PCIEx16

Size	Document Number
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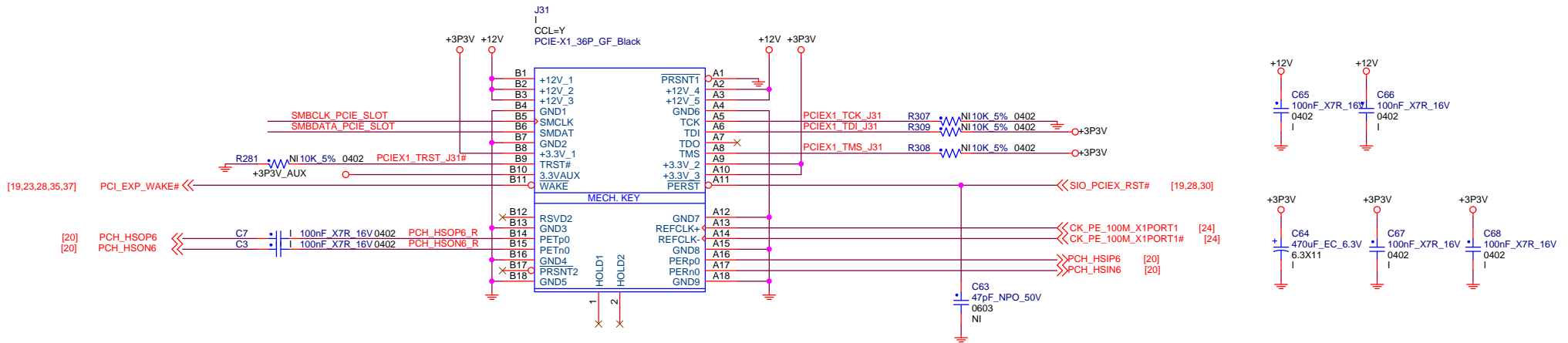
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Date: Tuesday, November 17, 2015

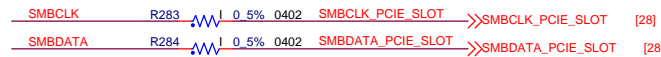
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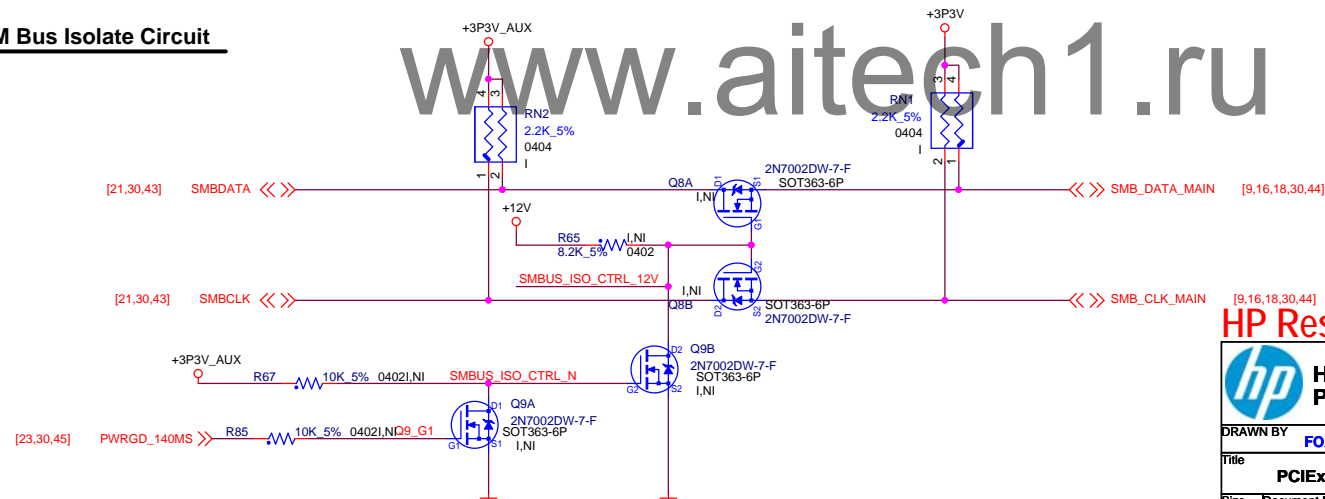
PCI EXPRESS X1 SLOT1



For Monotonic improve use

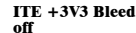


SM Bus Isolate Circuit



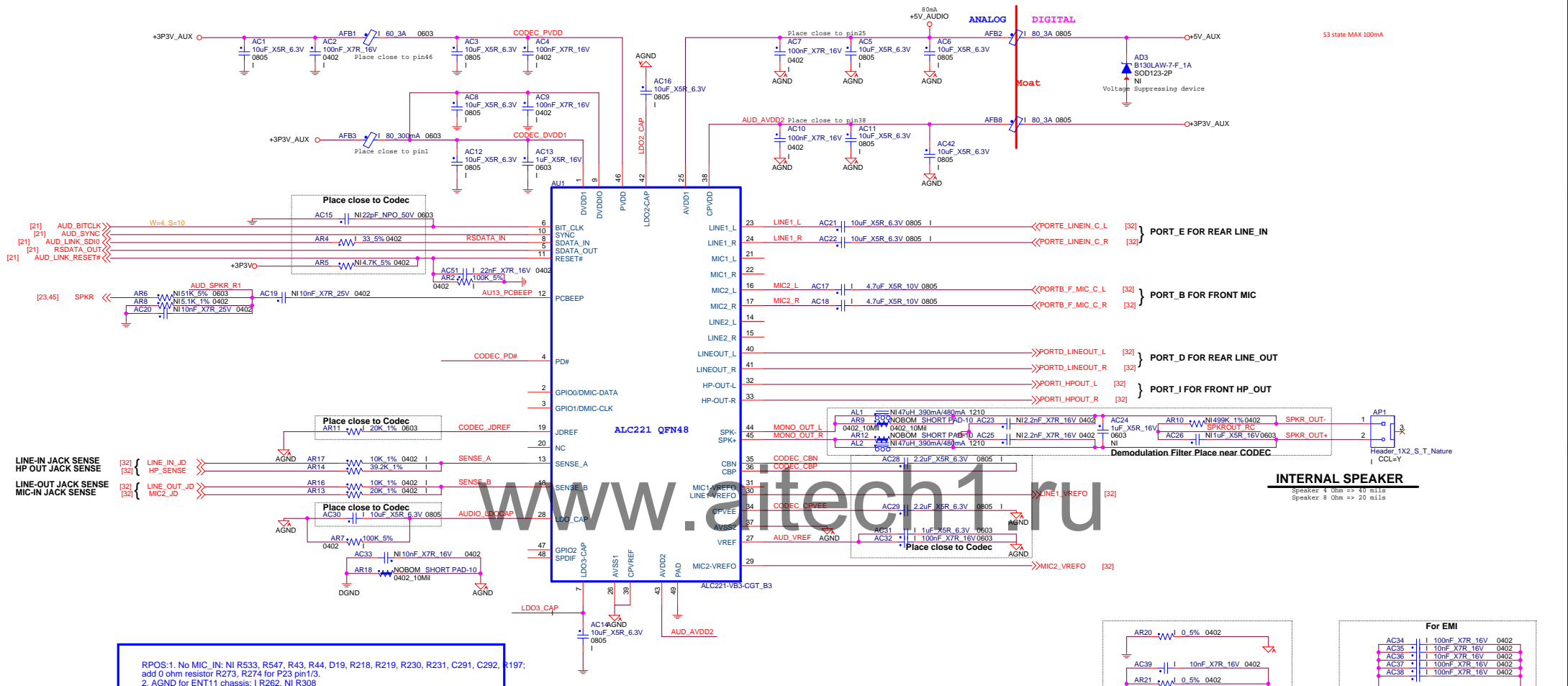
Power-On Strapping

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 6Bh default value always 80h)



HD AUDIO CODEC

+5V_AUDIO

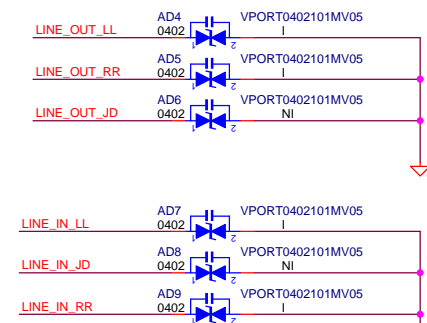
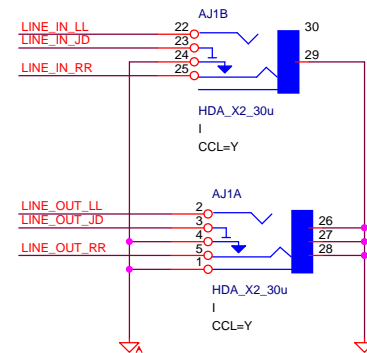




INTERNAL SPEAKER

Speaker 4 Ohm => 40 mls
Speaker 8 Ohm => 20 mls

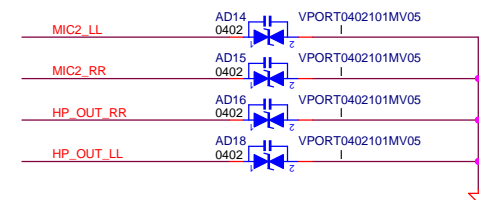
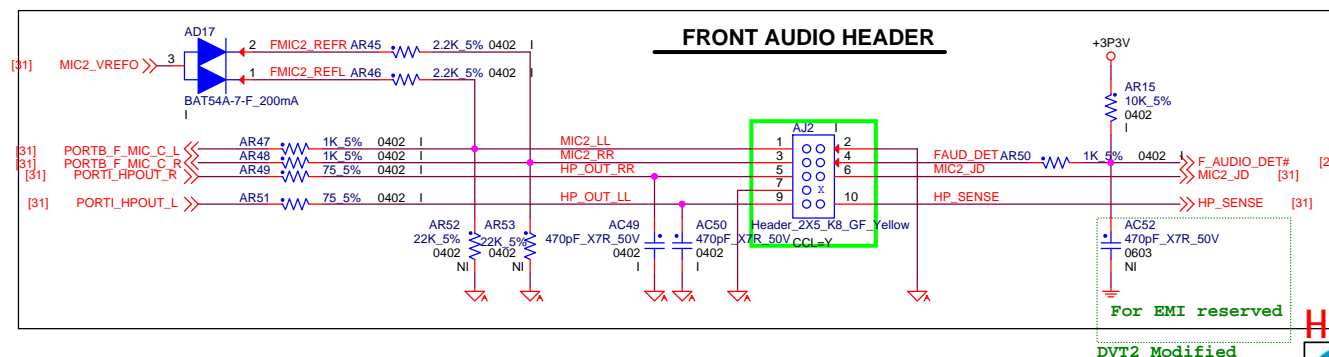
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Size: Document Number	Rev: 0.1
Customer: 828965-000	
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E		LINE_IN
D		LINE_OUT

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Title

AUDIO CONNECTOR

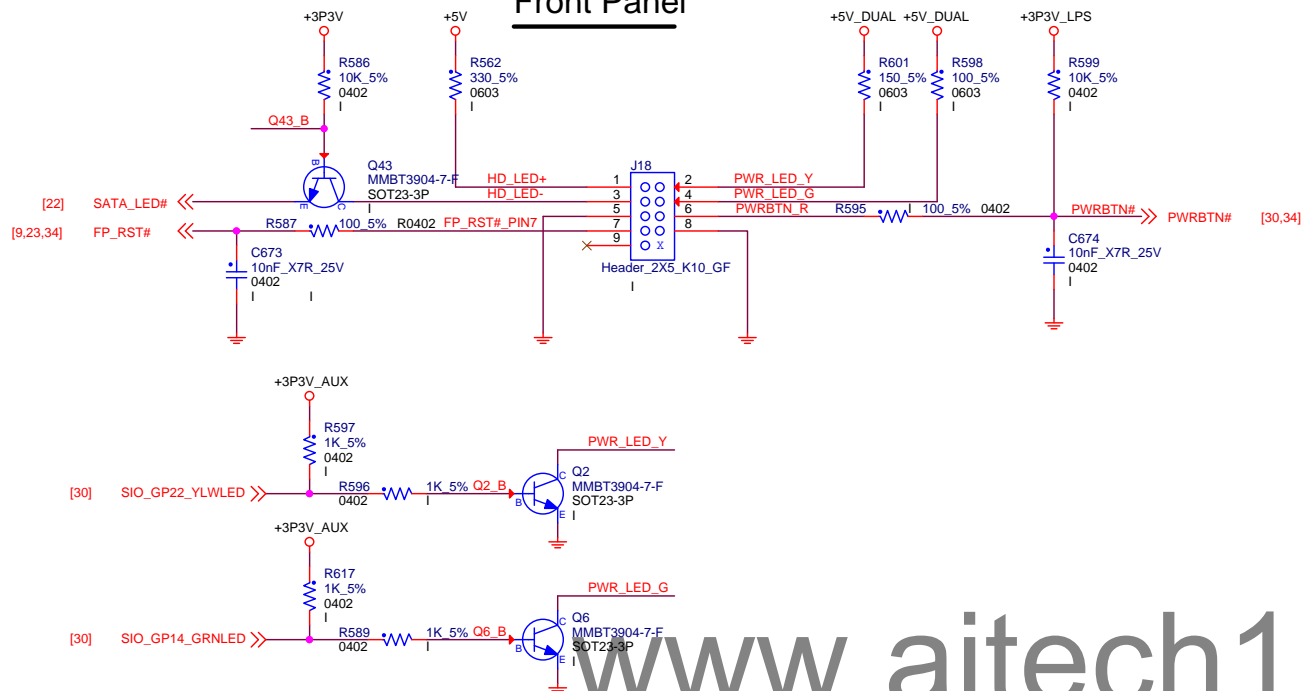
Size	Document Number
Custom	828985-000

Rev	0.1
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Date: Tuesday, November 17, 2015

Sheet	32	of	62
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Front Panel



HP Restricted Secret.


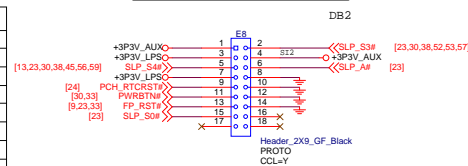
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		<small>THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS HEWLETT-PACKARD (HP). DO NOT DISCLOSE TO OR DUPLICATE OTHERS EXCEPT AS AUTHORIZED BY HP.</small>	
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Title FRONT PANEL			
Size B	Document Number 828985-000		Rev 0.1
Date: Tuesday, November 17, 2015	Sheet 33	of 62	



Table 27-4. Pin Location for Dual-in-Line header

Signal Name	Pin			Pin	Signal Name
VccSus3_3	1	o	o	2	SLP_3#
VccDSW3_3	3	o	o	4	SLP_5#
SLP_5#	5	o	o	6	SLP_A#
VccDSW3_3	7	o	o	8	GND
RTCRST#	9	o	o	10	GND (for RTCRST#)
PWRBTN#	11	o	o	12	GND (for PWRBTN#)
SVS_RESET#	13	o	o	14	GND (for SVS_RESET#)
SLP_S0#	15	o	o	16	NC
NC	17	o		18	NC

METS/APS TEST HEADER

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Title	SPI ROM & LPC DEBUG
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Size	Document Number
Custom	828985-000

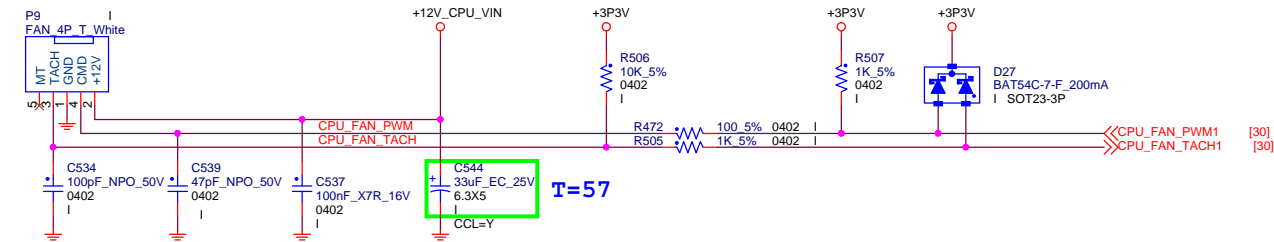
Rev	01
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Date: Tuesday, November 17, 2015 Sheet 34 of 62

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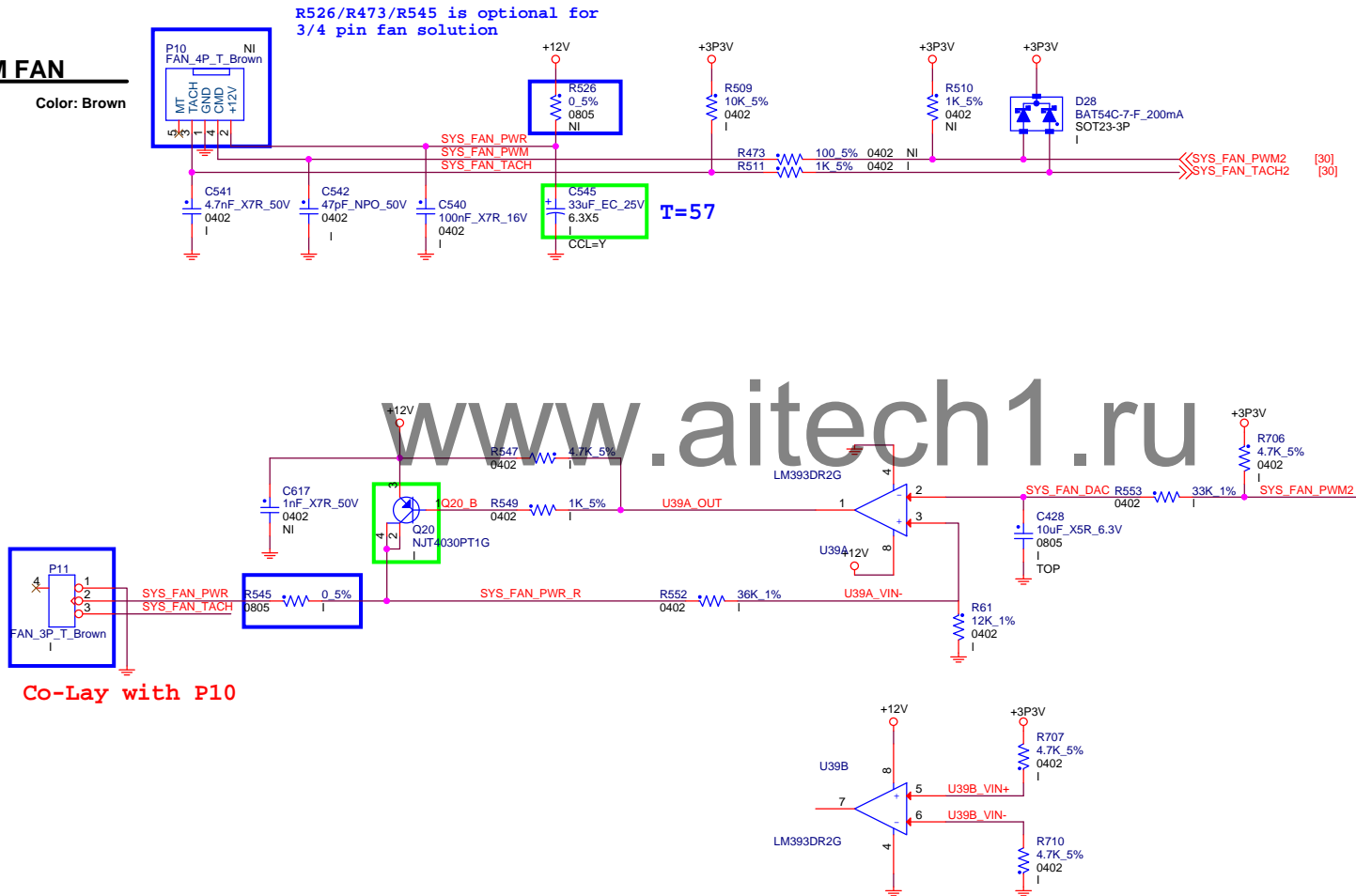
CPU FAN

Color: White




SYSTEM FAN

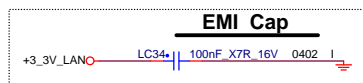
Color: Brown



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DRAWN BY FOXCONN					
Title FAN HEADERS					
Size	Document Number				Rev
Custom	828985-000				0.1
Date:	Tuesday, November 17, 2015	Sheet	36	of	62

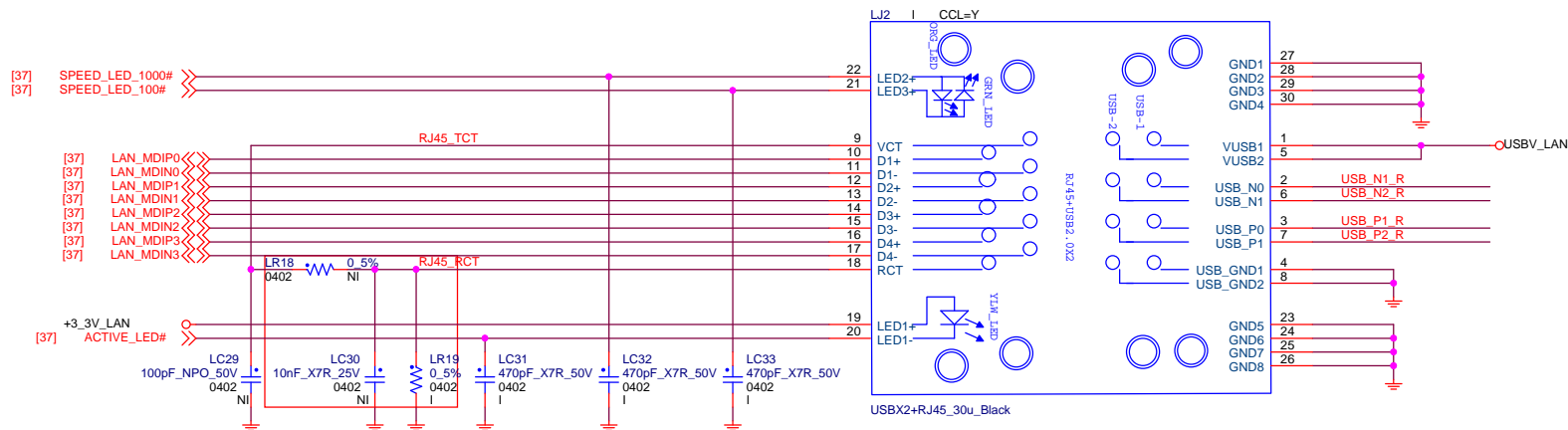
DORA DVT Modified



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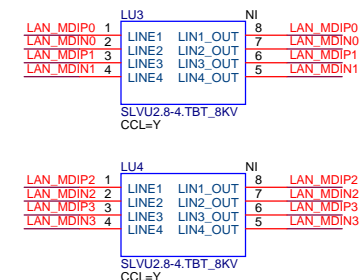
LR19 NI since pin18 has internally connect to GND

No Surge IC inside

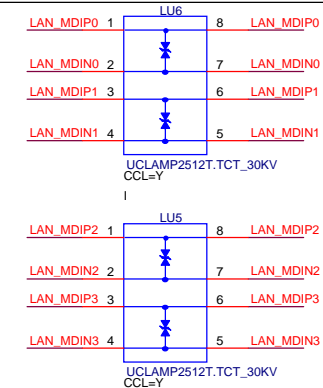
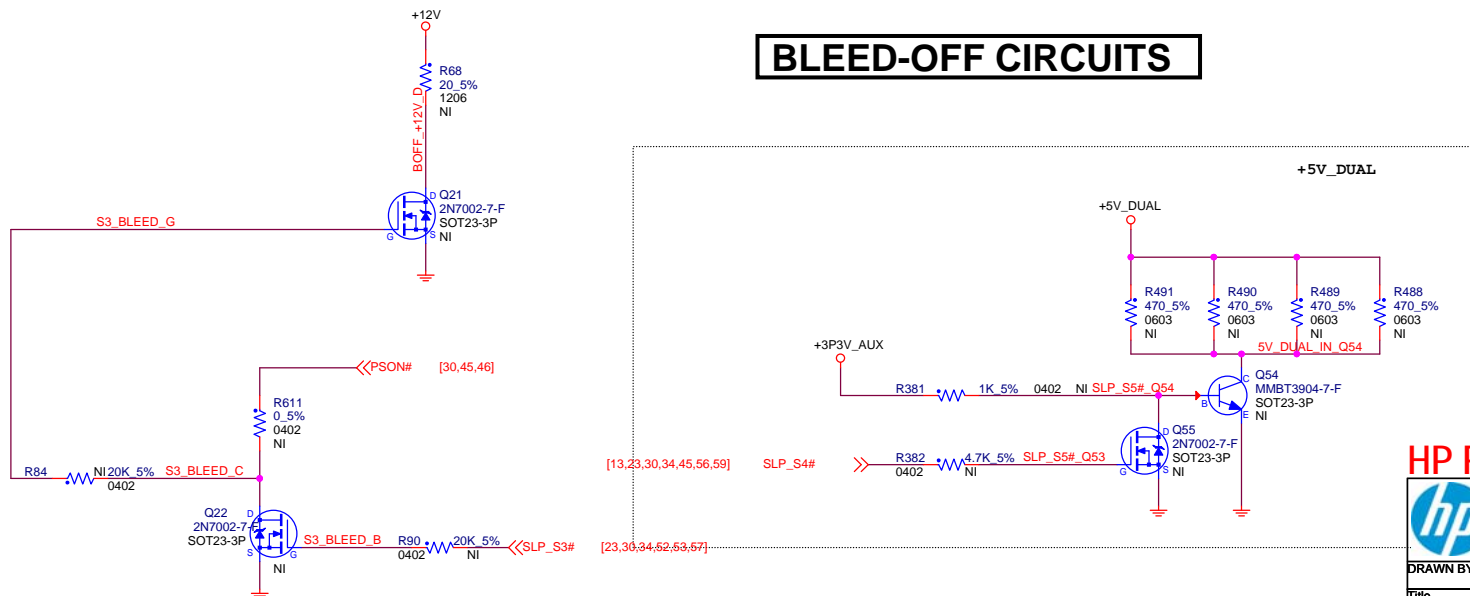
10/100M : LC30, LR18==> I, LR19 ==> NI
1000M : LC30, LR18 ==> NI, LR19 ==> I



Surge IC close to RJ45--CO-LAYOUT



BLEED-OFF CIRCUITS

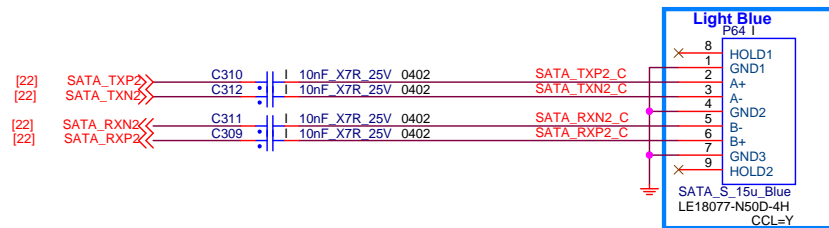
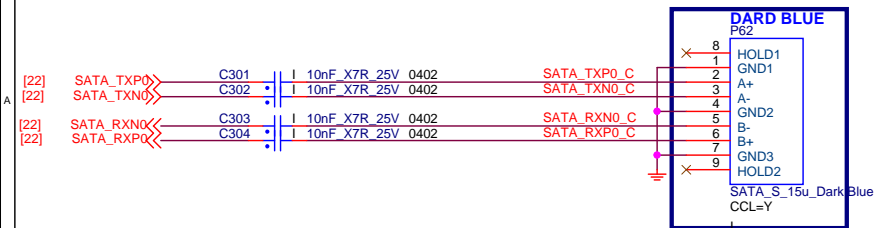


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Size	Document Number	Rev	
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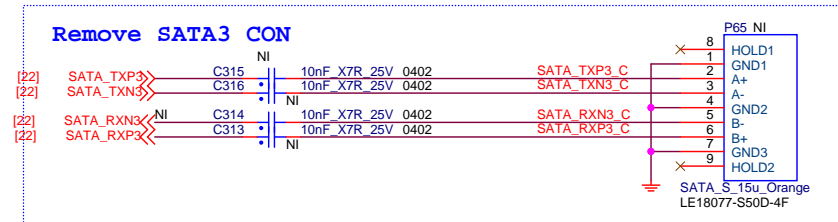
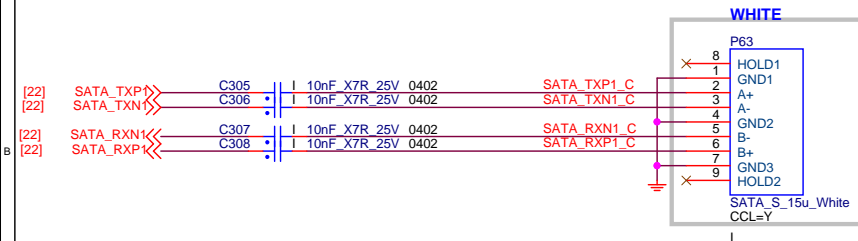
SATA 3.0 Port0.1

SATA 2.0 Port2.3

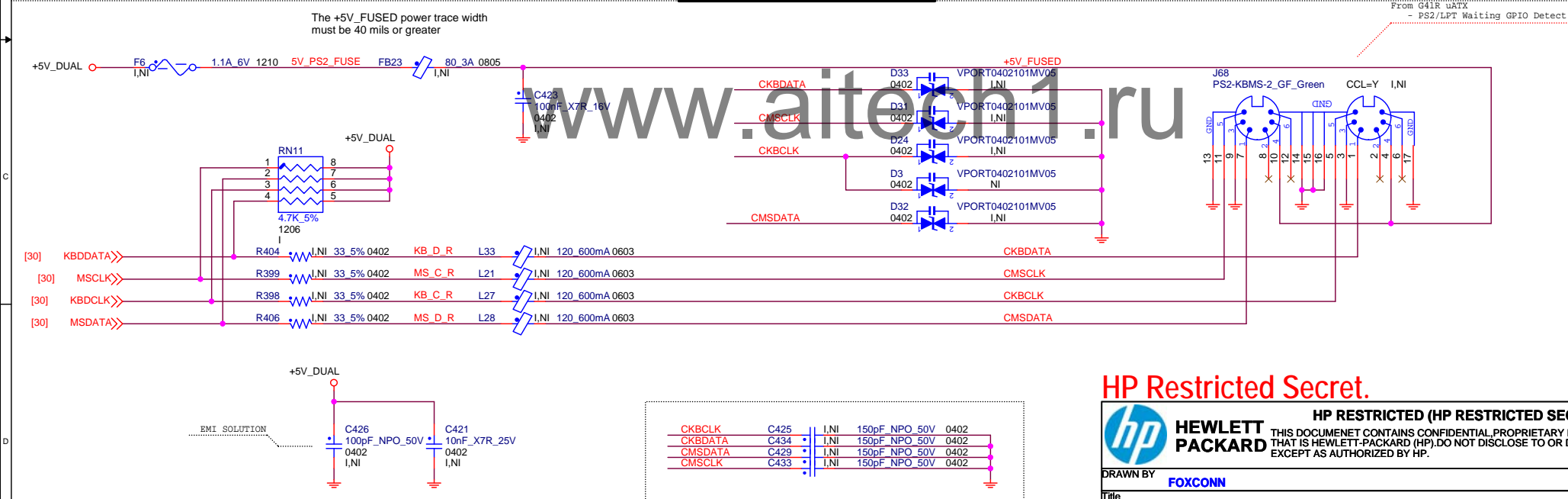


PVT Modified

Remove SATA3 CON

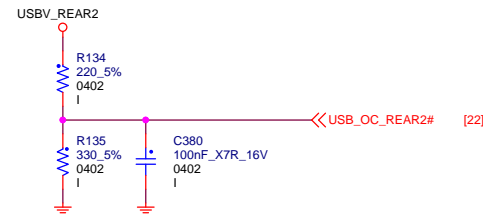
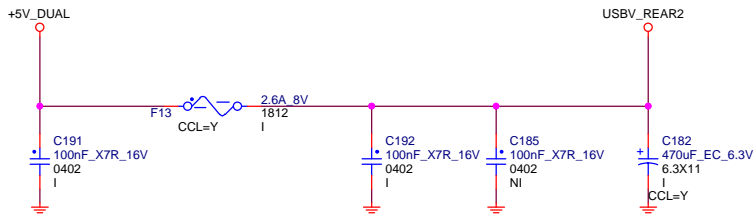
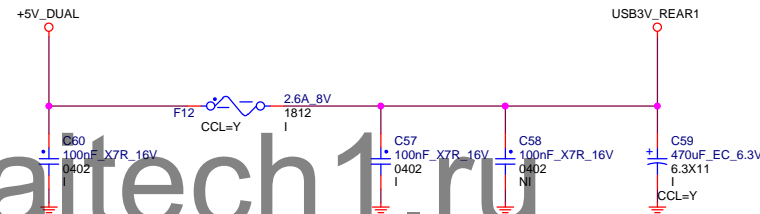
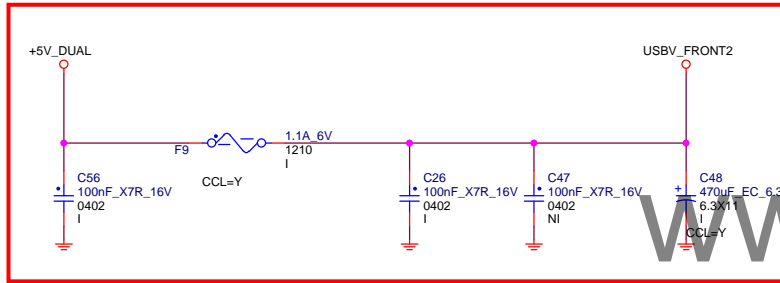
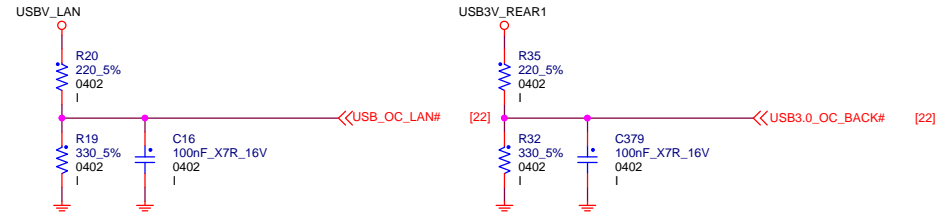
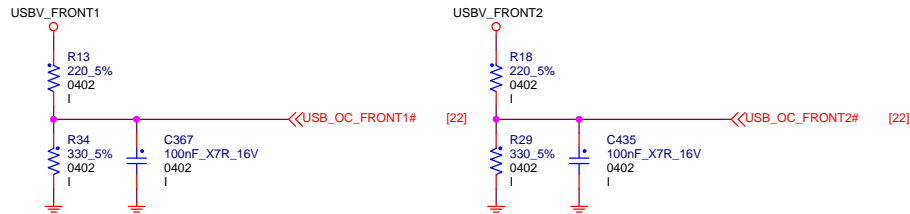
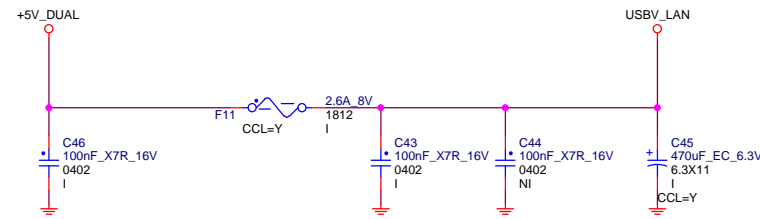
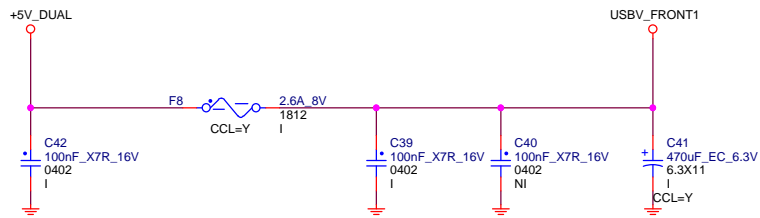


KEYBOARD / MOUSE



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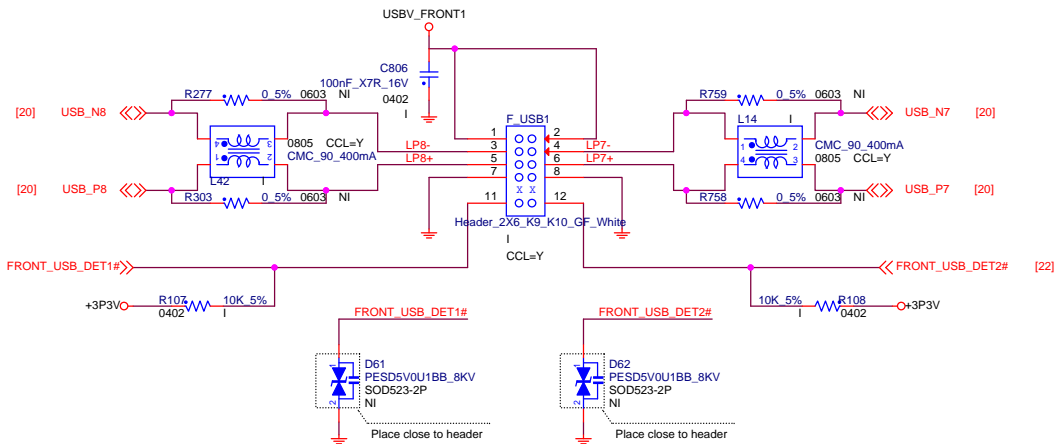
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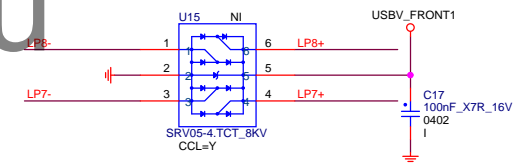
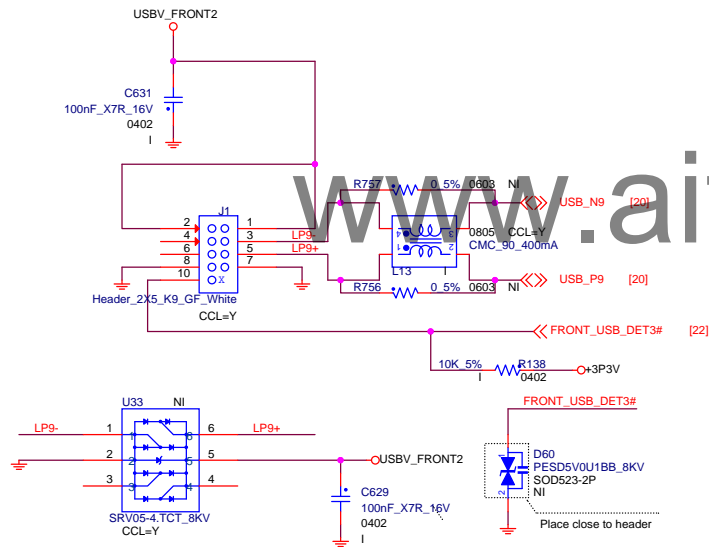
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Front USB2.0



Internal USB2.0



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Title

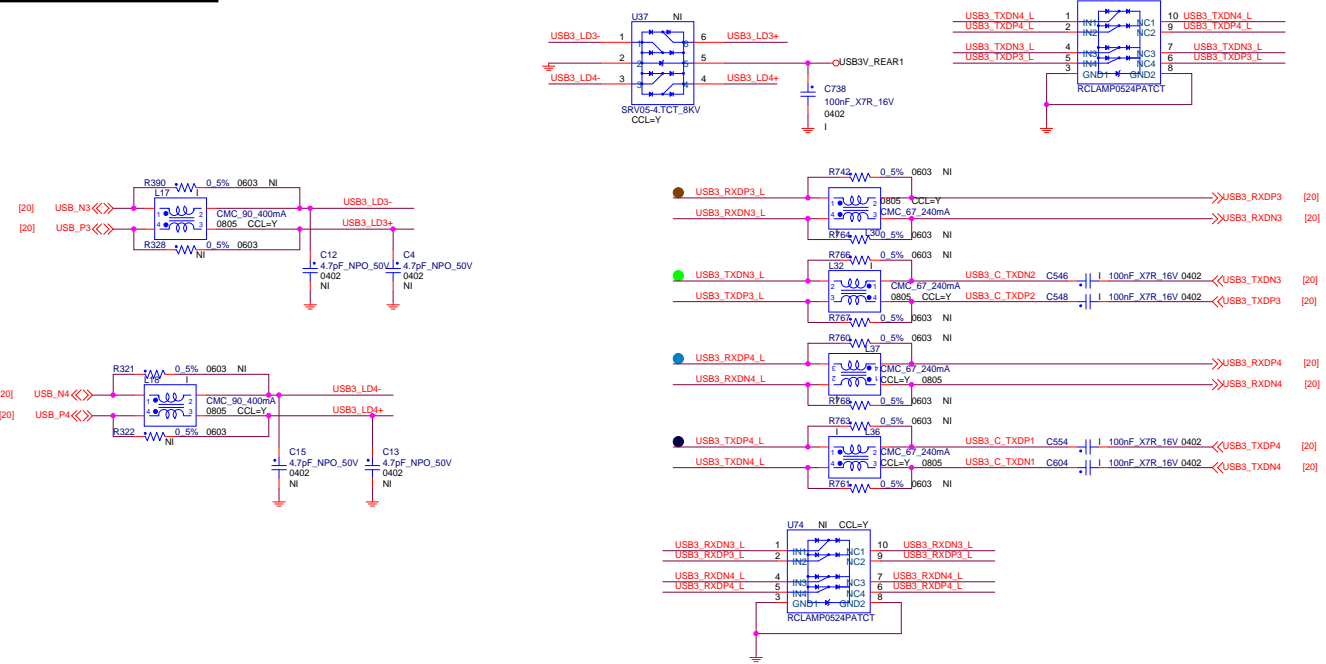
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Size	Document Number
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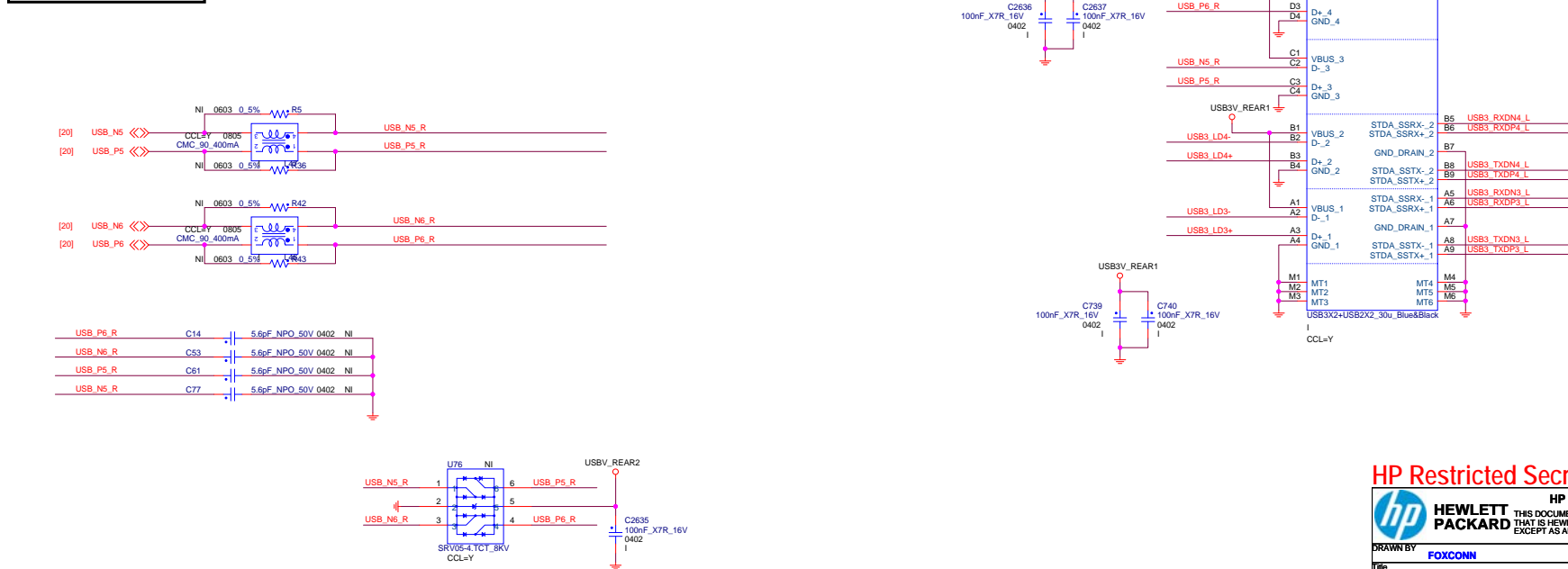
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REAR USB 3.0



REAR USB 2.0



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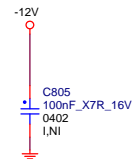
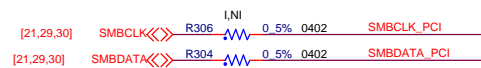
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Size: **C** Document Number: **828985-000** Rev: **0.1**

Date: **Tuesday, November 17, 2015** Sheet: **42** of **62**

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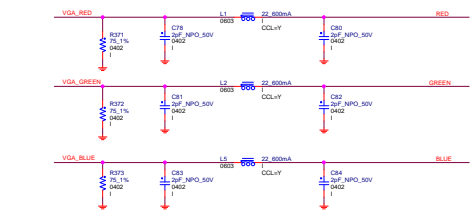
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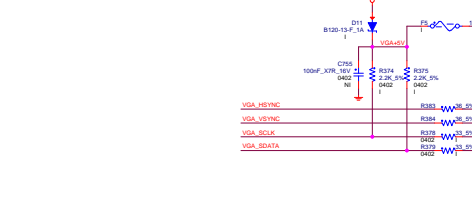
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Title	PCI SLOT
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Rev
0.1

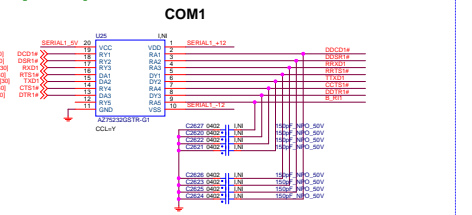


Place 150 ohm resistors close to filters (Cap/Ferrite-Beads)

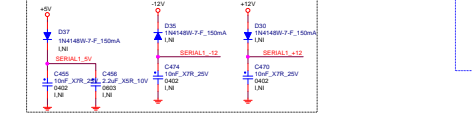


DORA DVT Modified

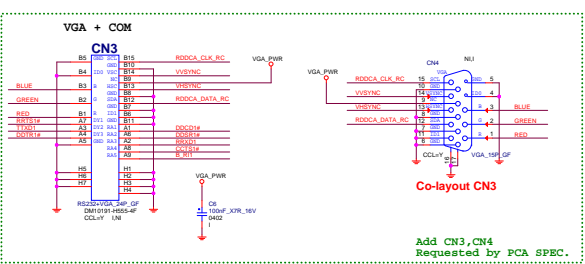
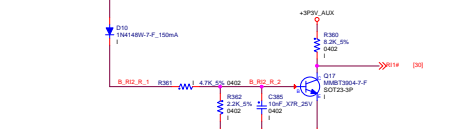
Add COM1,COM2,follow sharan schematic Requested by PCA SPEC.



Place caps close to U25



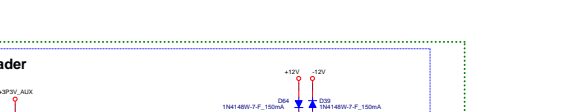
Place caps close to U25



Add CN3,CN4 Requested by PCA SPEC.



Co-layout CN3



Co-layout CN3



Co-layout CN3



Co-layout CN3



Co-layout CN3



Co-layout CN3

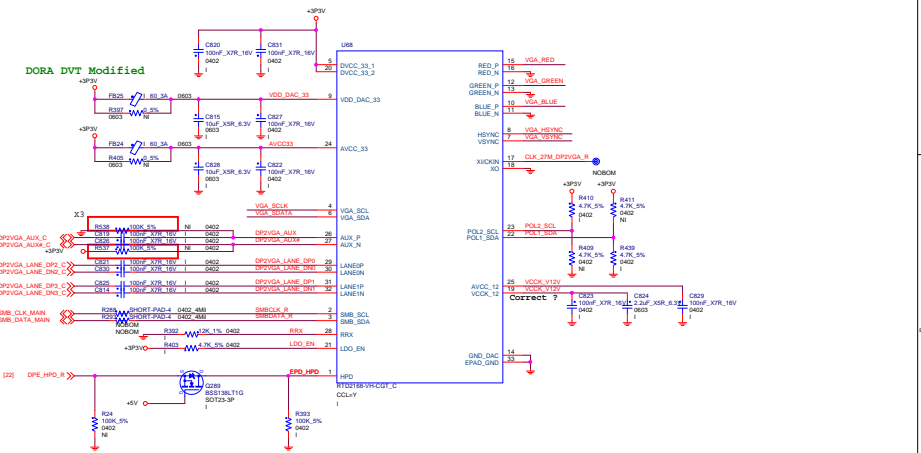


Co-layout CN3

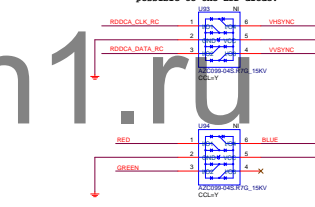


Co-layout CN3

DP to VGA RTD2168



WSD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the BSD diode.



WSD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the BSD diode.



WSD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the BSD diode.



WSD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the BSD diode.



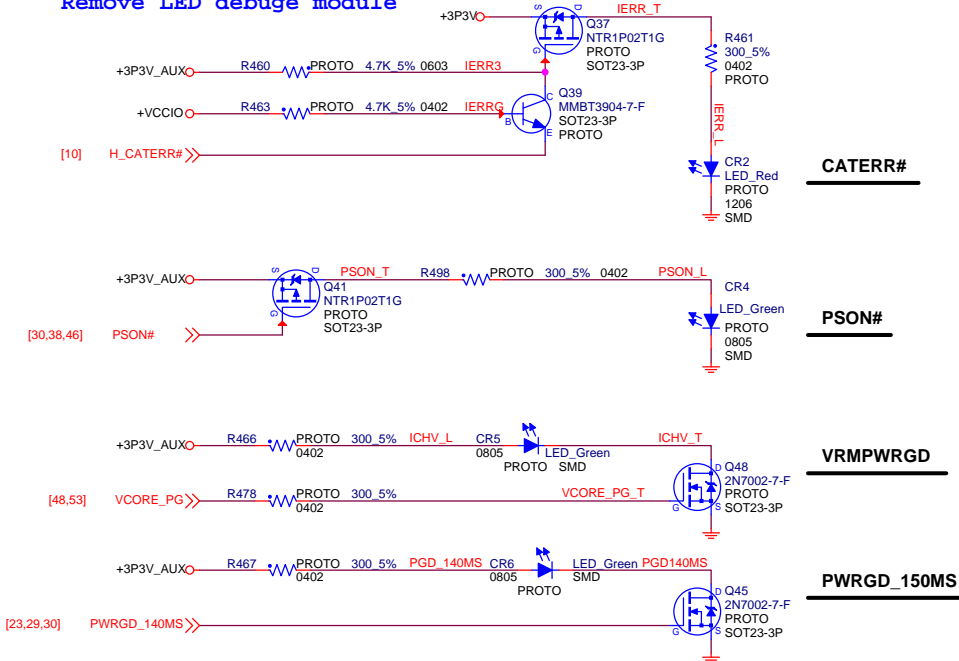
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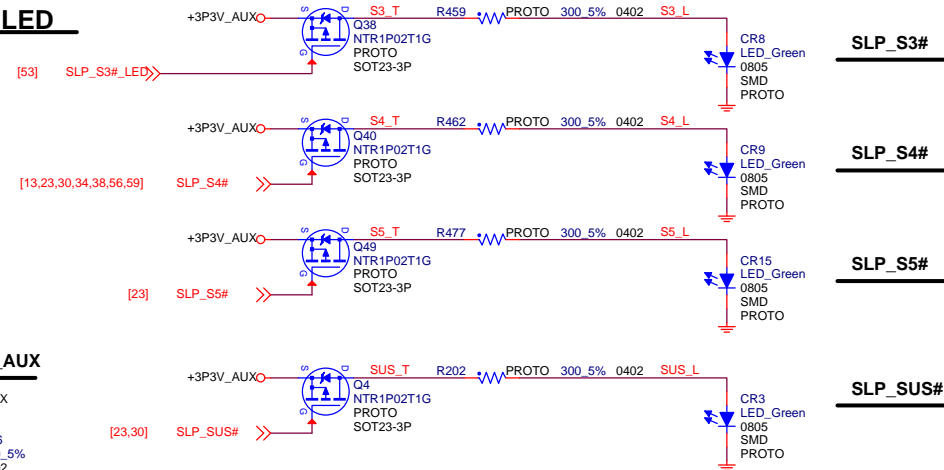
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Rev	00000000
D	00000000
Rev	00000000

PVT Modified

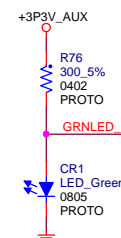
Remove LED debug module



PCA LED



+3P3V_AUX

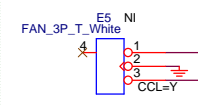


HOOD SENSE CIRCUIT

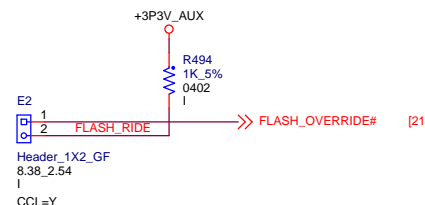
Have to take care the location

PVT Modified

Remove HOOD SENSE

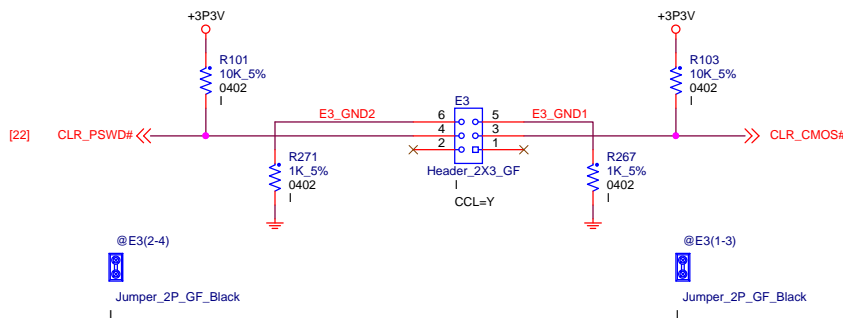


FLASH OVERRIDE (ME Disable)

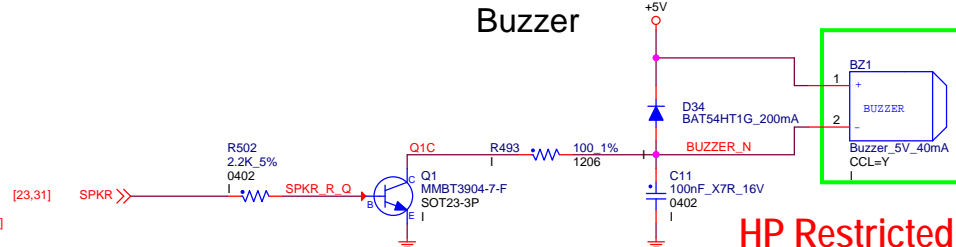


CLEAR PASSWORD

CLEAR CMOS



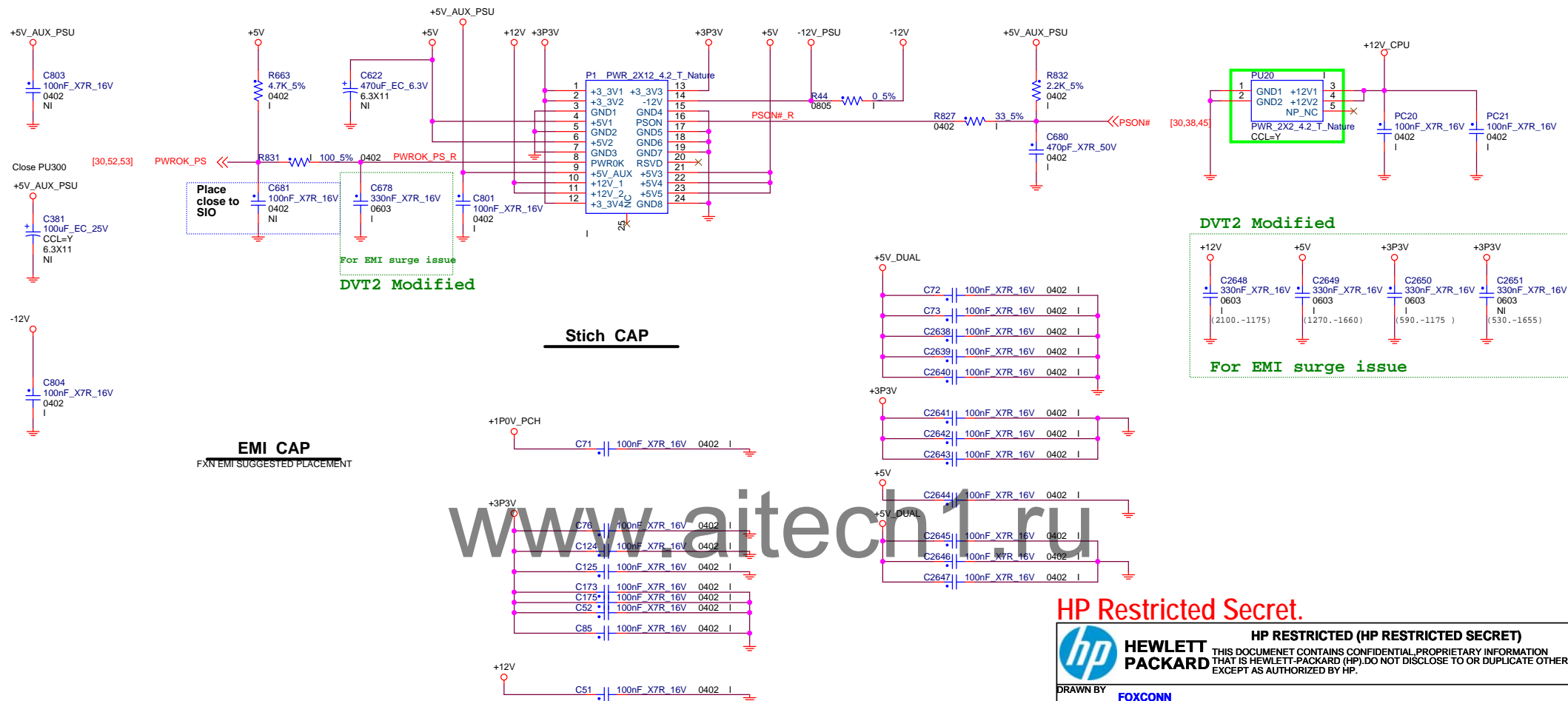
Buzzer



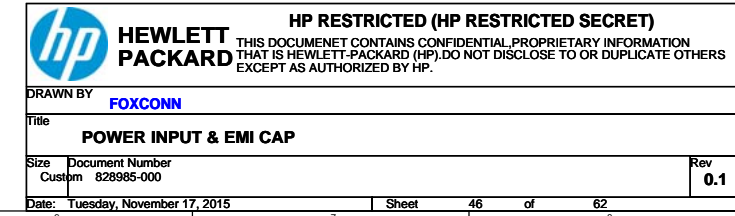
HP Restricted Secret.

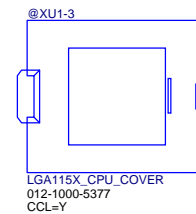
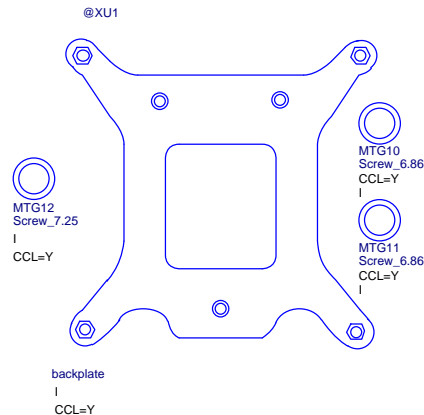
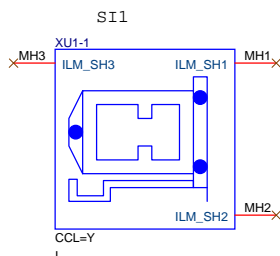
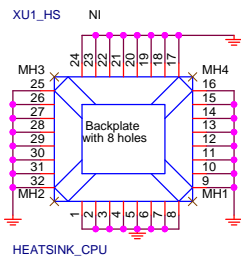
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Size	Document Number	Custom		Rev	
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Power Input Connector



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ILM & SCREWS

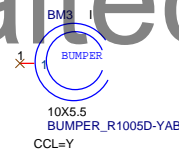
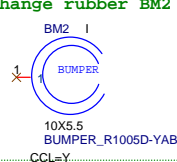
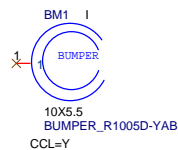
Licence Label

PCB

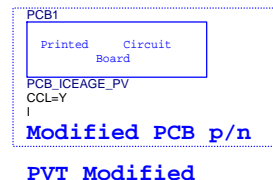
Modify Note:
- PCB Information
- PCB Stack-up information

DORA DVT Modified

Change rubber BM2 to 7D050FG00-R60-B from 7D0617100-G1G-G

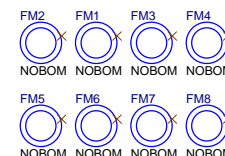
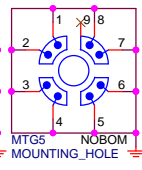
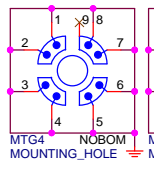
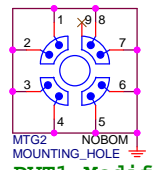
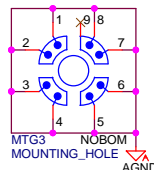
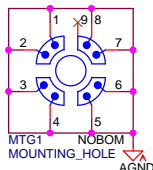


Note:
BIOS_LICENCE
AMI uEFI



Modified PCB p/n

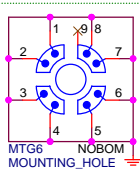
PVT Modified



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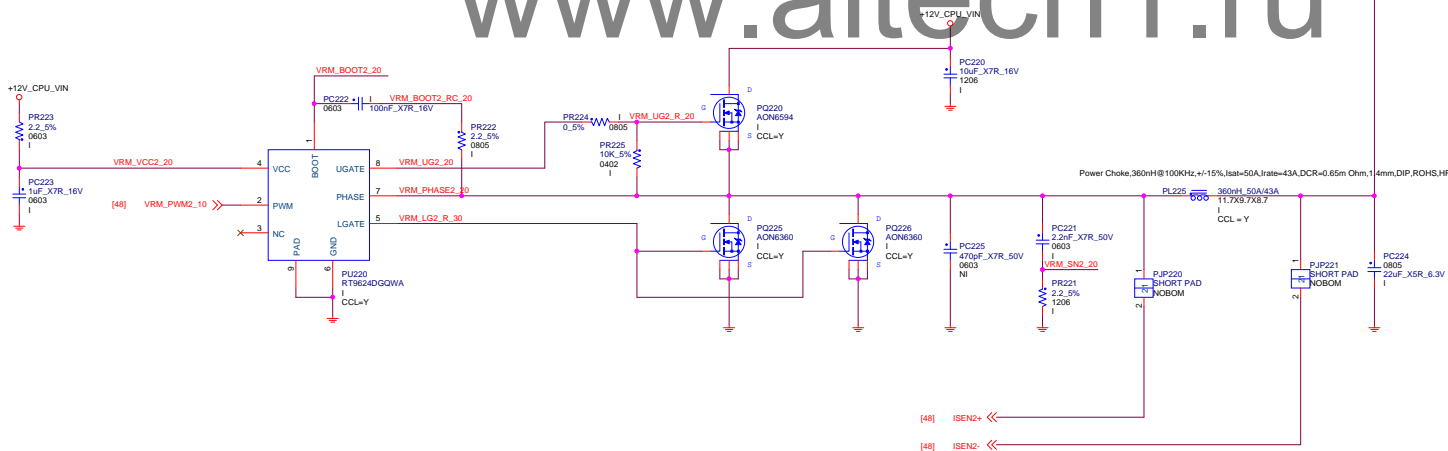
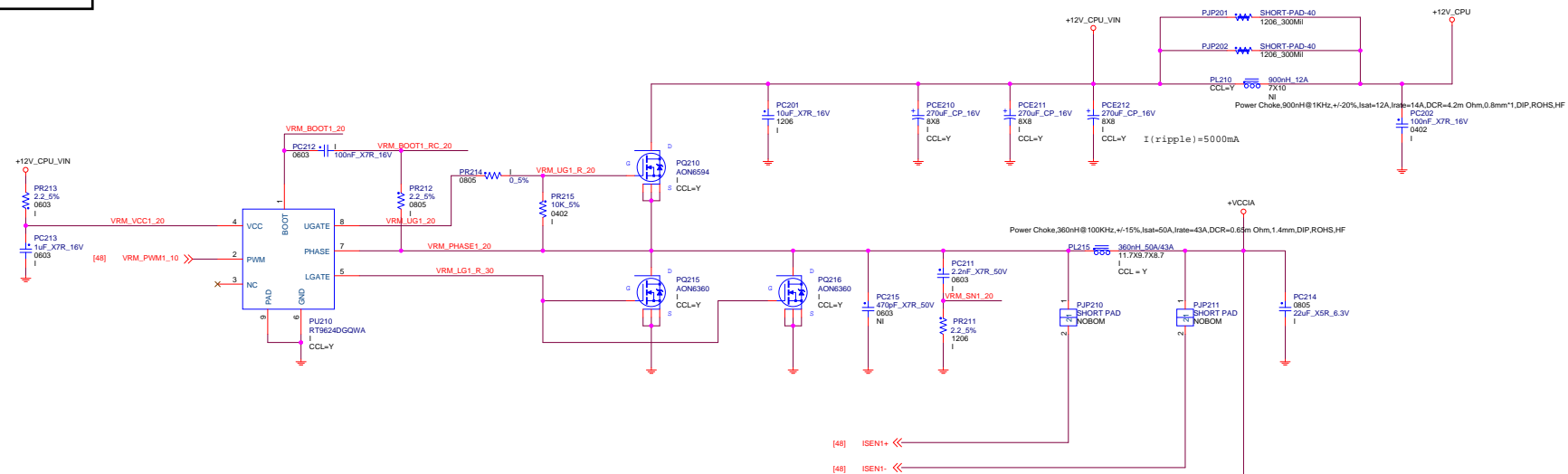
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Title PCB/MECHANICAL PARTS			
Size	Document Number	Rev	
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Date:	Tuesday, November 17, 2015	Sheet	47 of 62

Add MTG6 to meet uATX spec.



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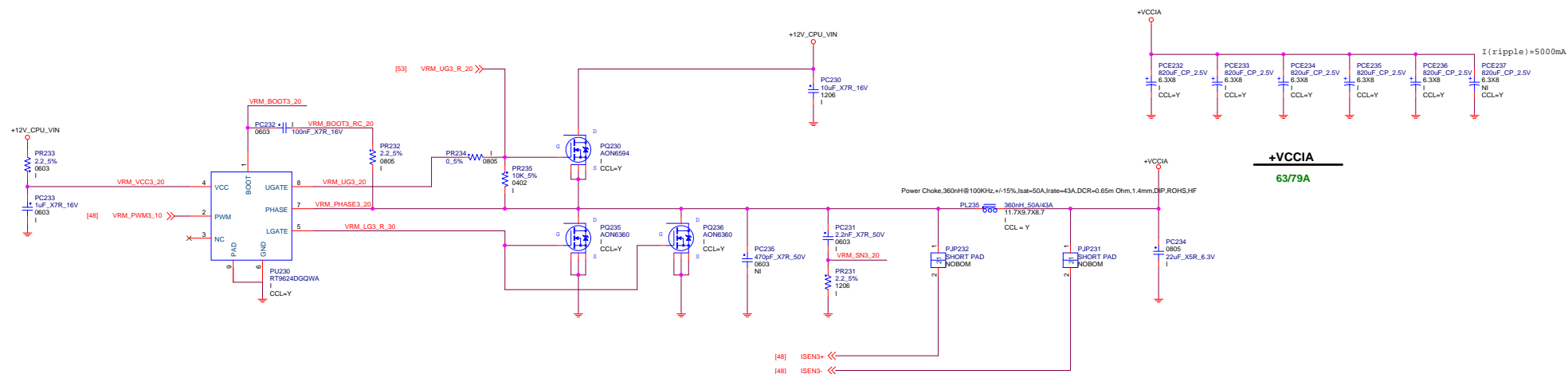
VCORE PHASE1~2



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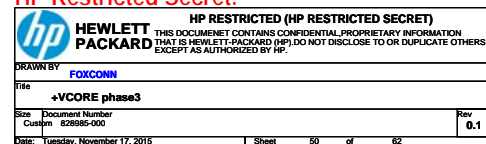
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VCORE PHASE3



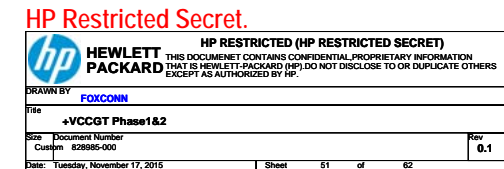
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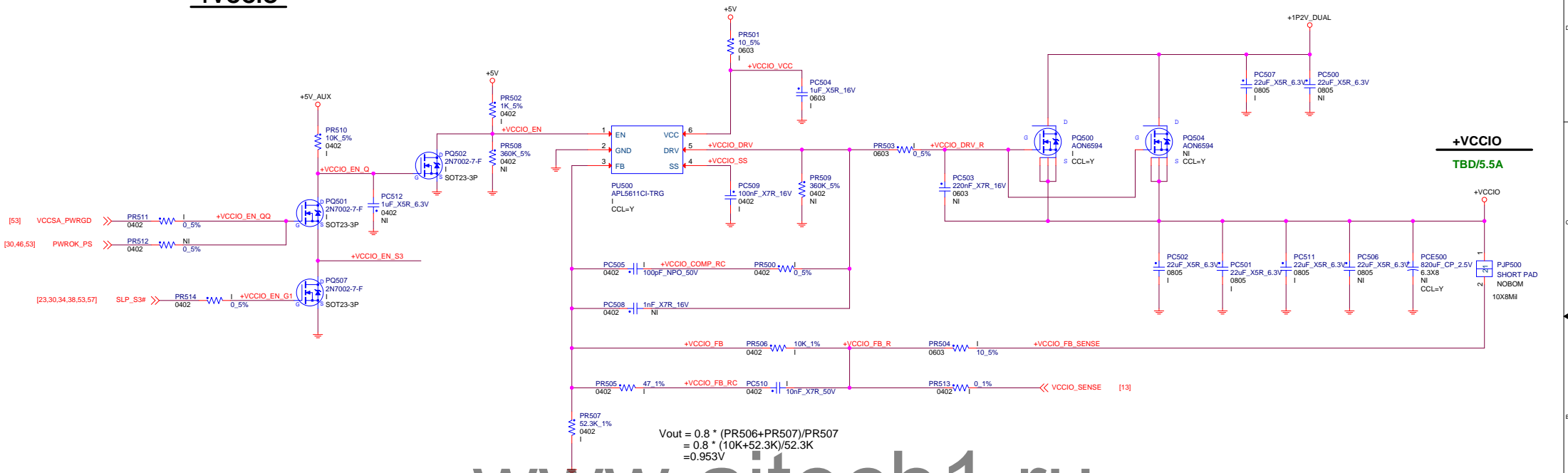


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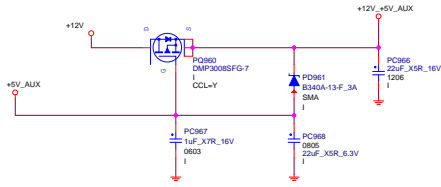
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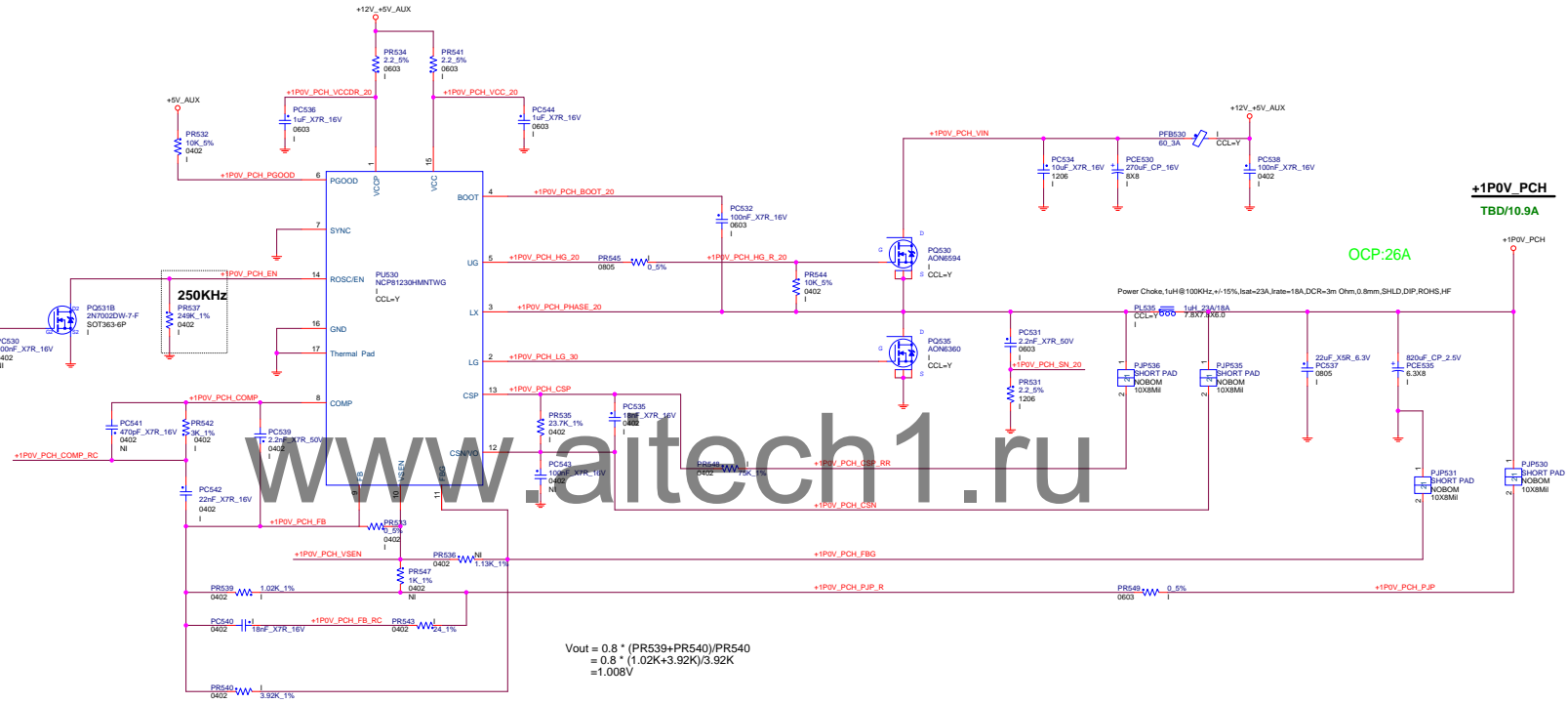
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+12V_+5V_AUX



+12V_+5V_AUX TBD/TBD



$$V_{out} = 0.8 * (PR539 + PR540) / PR540$$

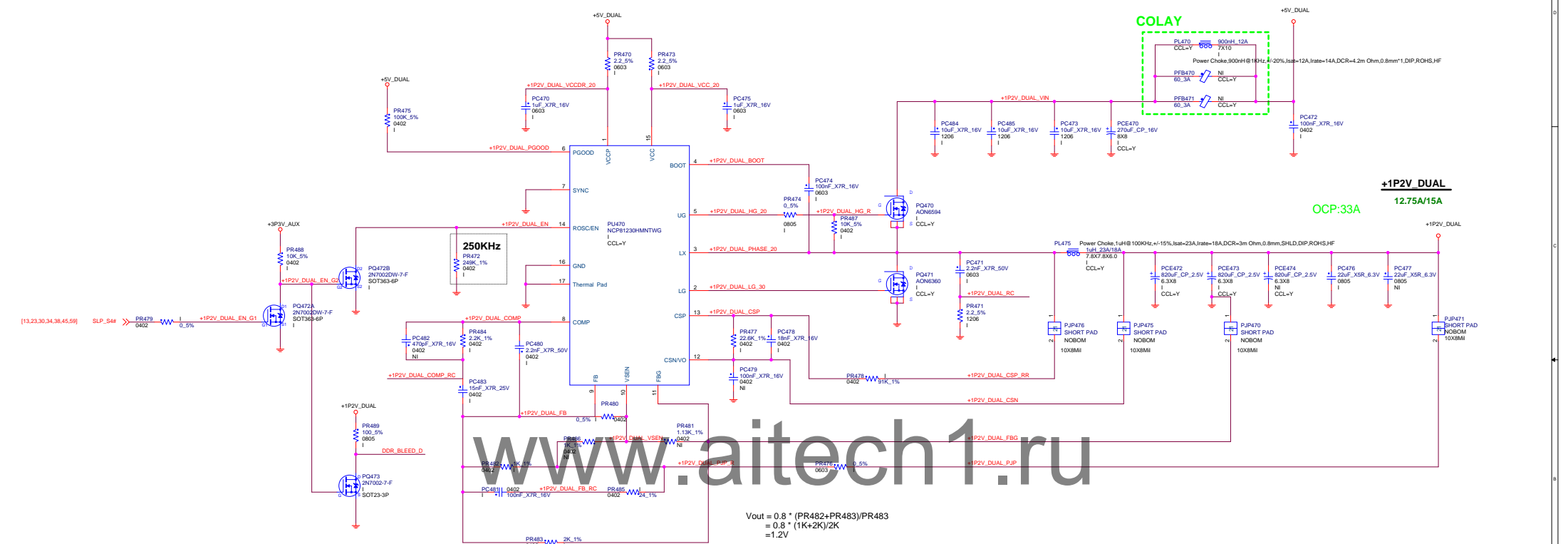
$$= 0.8 * (1.02K + 3.92K) / 3.92K$$

$$= 1.008V$$

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P/B: +1P0V_PCH			
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+1P2V_DUAL POWER(DDR 4)



$$V_{out} = 0.8 \cdot (PR482 + PR483) / PR481$$
$$= 0.8 \cdot (1K + 2K) / 2K$$
$$= 1.2V$$

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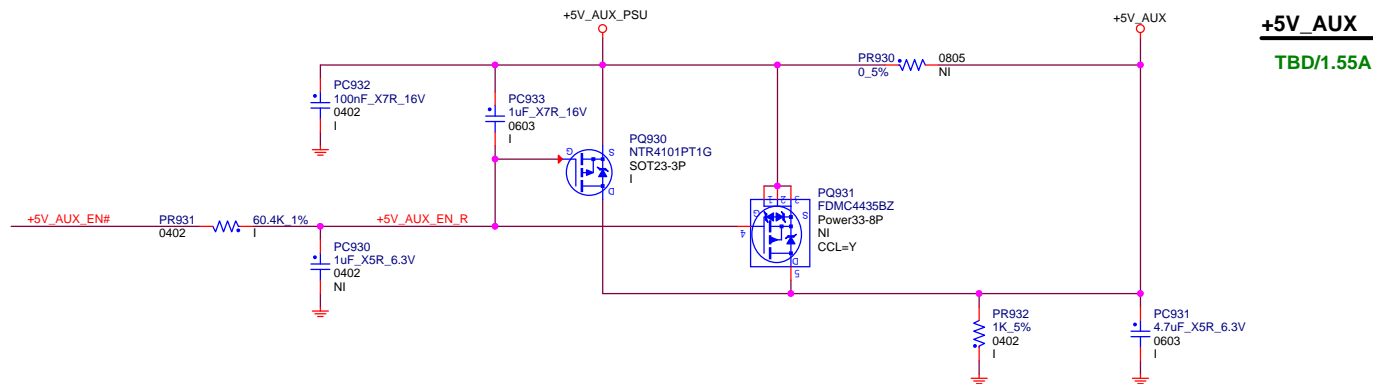
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DDR_VTT



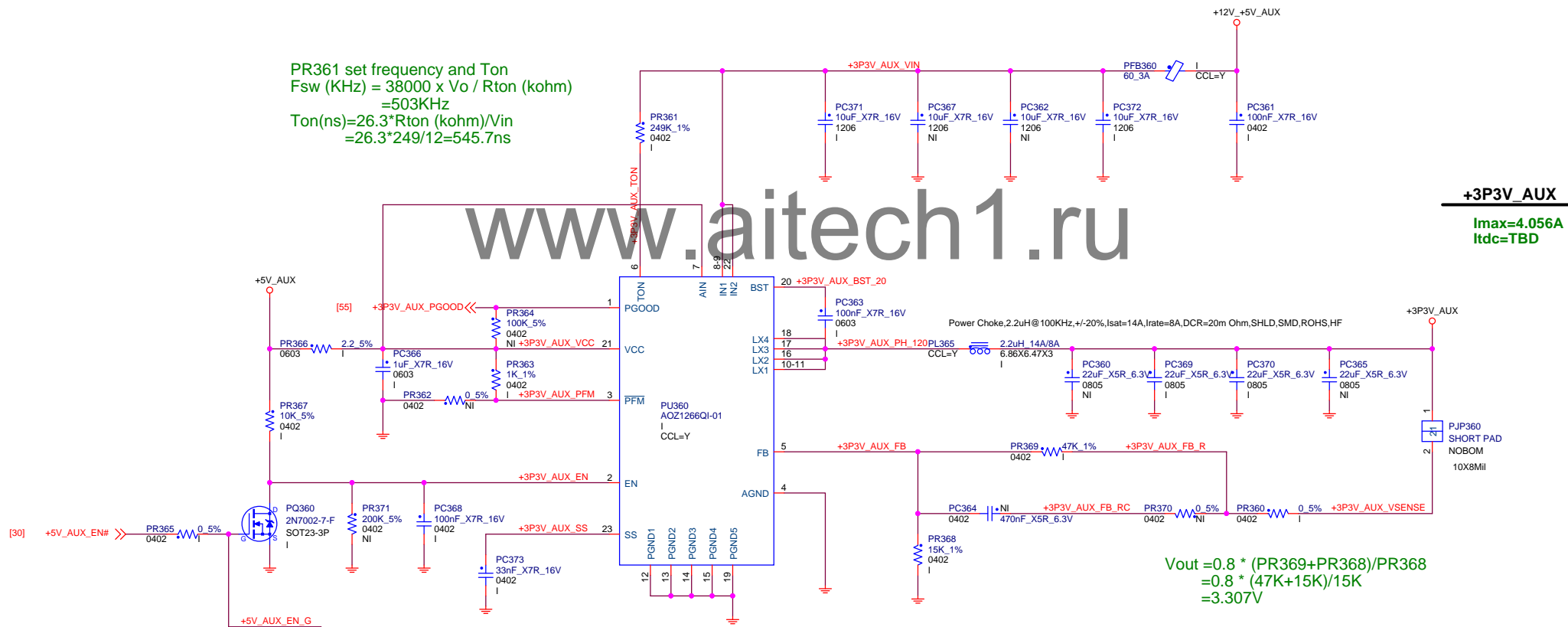
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+5V_AUX
TBD/1.55A

PR361 set frequency and Ton
 $F_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$
 $= 503 \text{ KHz}$
 $Ton \text{ (ns)} = 26.3 \times R_{ton} \text{ (kohm)} / V_{in}$
 $= 26.3 \times 249 / 12 = 545.7 \text{ ns}$

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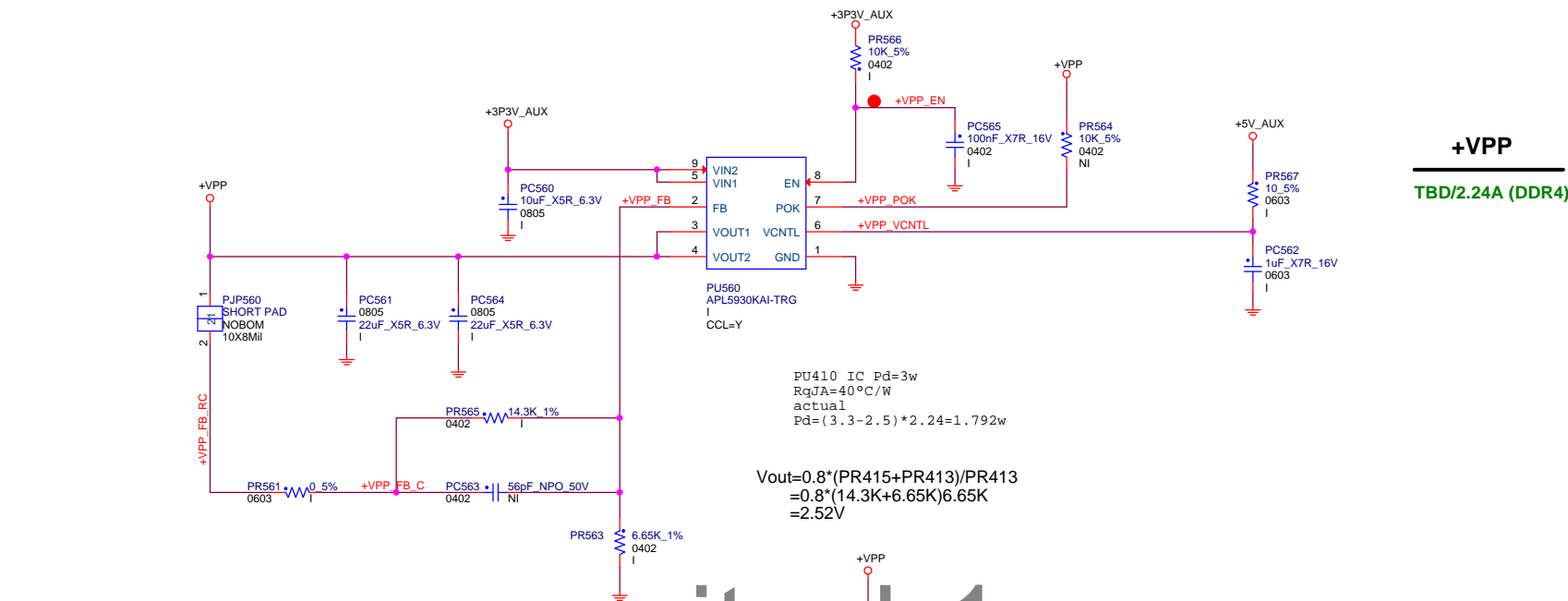


+3P3V_AUX
 $I_{max} = 4.056 \text{ A}$
 $I_{dc} = \text{TBD}$

$V_{out} = 0.8 \times (PR369 + PR368) / PR368$
 $= 0.8 \times (47K + 15K) / 15K$
 $= 3.307 \text{ V}$

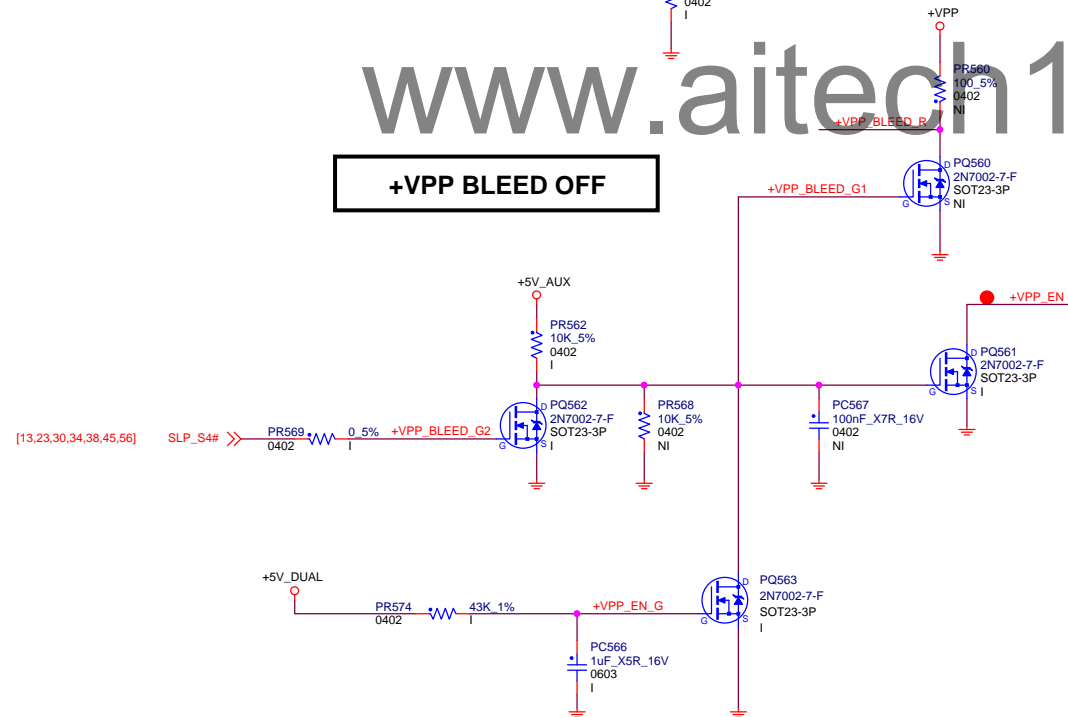
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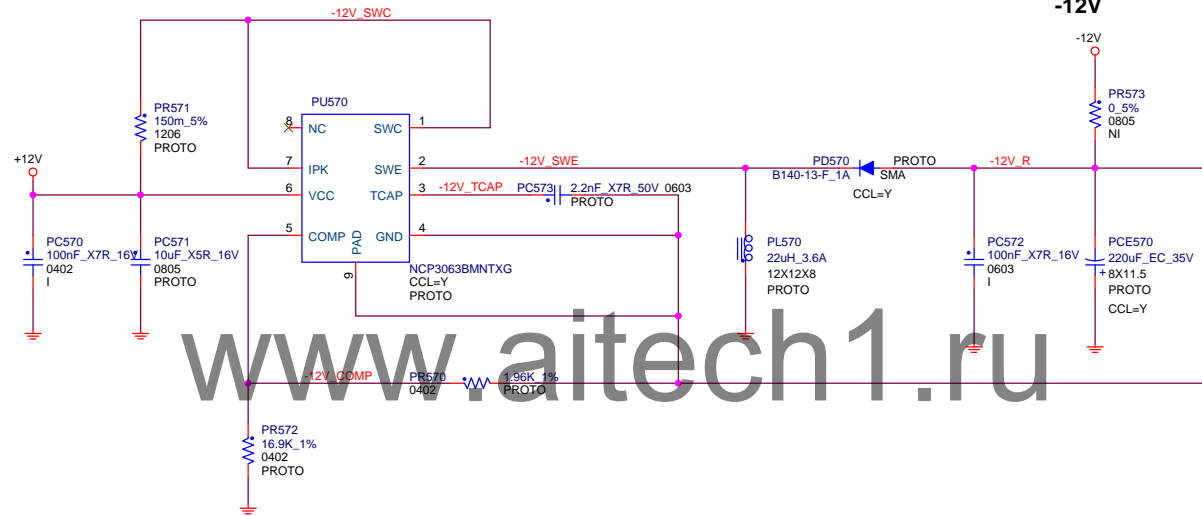
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-12V




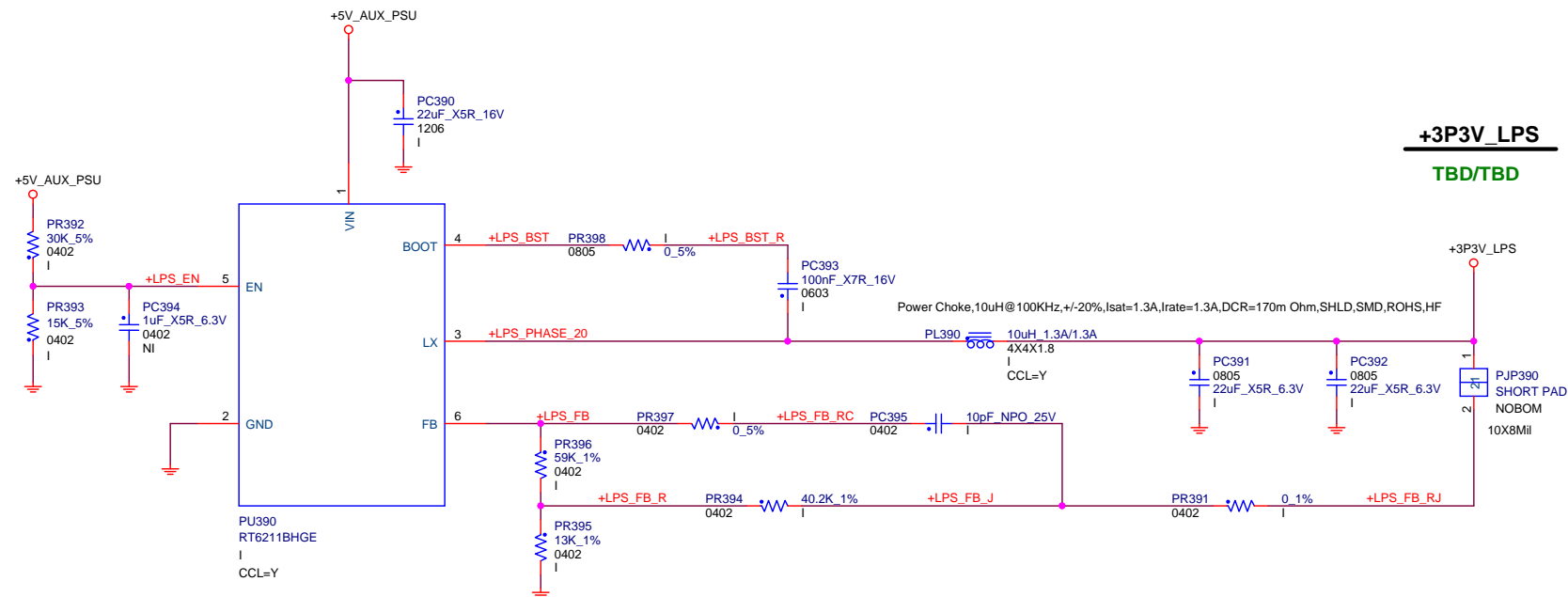
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-12V

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Change List

ICEAGE_SCHEMATIC_X1_2015_0330_1540-MULTI OPT.DSN

- 1:Change the M2_2230 module from I to NI
2:Change the PCB size to 9.2*8.6

- 20150414
1:Change the PCB size to 9.3*8.9
2:Change R838,R835 to I follow CRB require POR
3:Change SR215 to 43ohm follow PECl design guide
4:Add serial resister R147 for LPC CLK

- 20150415
1:Update block diagram, clock diagram
2:Change C684 to 100nf for M2 power decoup
3:Update audio schematic follow vendor's suggestion

- 20150426
1:Add board ID(0-2) and board SKU(0-1) at page23
2:Change cpu back plate to FOXCONN_PW35311-004

- 20150505
1:Change TPM to SLB9670VQ1.2FW6.40

- 20150511
1:Change C205 to I--intel require
2:change C181,C178 to 2.2uf,add C102 2.2uf reserve--intel review
3:Change R343,R344 to NI--intel review
4:Change J1 to 2x5 header for HP requirement
5:add C103,C104 0805 22uf and C88,C89,C98 0606 22uf for VCCIA --intel review
6:Add C99,C105,C106 0805 47uf outside and C100,C101 in cavity--intel review
7:add C599 0805 22uf for VCCIO--intel review
8:Change C205 to I--intel review
9:Change C178, C181 to 2.2uF, +1P0V_VCCAPLL_FB_R reserve 1*2.2uF--intel review
10:Change R343,R344 to NI ---intel review

DB to Pre-SI change List

- 20150605
1.Change J1 from L&S_2301014210 2x5_k10 to FOXCONN_HC11051-WP9 2x5_k9 to match with card reader---SIO1171562
20150609
1.Add SIO_TPM_RST# connect from SIO to TPM reset for TPM no function issue---
20150611 DC change
1.For +VCCIO voltage level issue Change PR507 to 52.3K
20150622 change
1.modify CPU/SYS fan from FAN CTRL1/2 to FAN CTRL2/3
2.PCH update to D1 version GLH110-QJHR

- 20150623 DC change
1.For +1P35V_DUAL voltage level issue Change PR484 to 2.2K_1%_0402 Change PC483 to 15nF_X7R_25V_0402 Change PC481 to 100nF_X7R_16V_0402
2.For VCCIA&VCCGT VCCIA PC114, PC144, PC146 change to 470nF_X7R_16V_0603 PR195, PR197, PR199 change to 1.37K_1%_0402 PC101 change to 220pF_NPO_50V_0402 PC102 change to 82pF_NPO_50V_0402 PR174 change to 6.98K_1%_0402

- VCCGT PC148, PC150 change to 470nF_X7R_0603_16V PR101, PR103 change to 1.4K_1%_0402 PC104 change to 220pF_NPO_50V_0402 PC103 change to 82pF_NPO_50V_0402 PR111 change to 17.4K_1%_0402 PR144 change to 10.7K_1%_0402 PR113 change to 13.3K_1%_0402 PR139 change to 29.4K_1%_0402 PR118 change to 165K_1%_0402 PR186 change to 3.01K_1%_0402 PR183 change to 698 ohm_1%_0402
3.For +VCCIO voltage level issue Change PR505 to 47 ohm_1%_0402
20150630 DC change
1.For +VCCSA Phase and Gain Margin issue Change PR618 to 100_1%_0402 Change PC612 to 1.5nF_X7R_50V_0402

- 20150701 DC change
1.For +1P35V_DUAL noise issue Add PL470,PFB470,PFB471,PFB530
2.+3P3V_AUX Change solution
3.PU302 change to UPI_UP0104TDDA

- 20150702 DC change
1.For +1P35V_DUAL noise issue Remove PCE471 Add PC484,PC485

- 20150702 EE change
1.change R229 from 0ohm to 33ohm for SLP_S4# monotonic issue---SIO1186076
2.change R201 from 10ohm to 33ohm for SLP_SUS# monotonic issue---SIO1186133
3.change C956,C8,C870 from 4.7uf to 10uf for vref DQ&CA fail issue---SIO1180412
4.change c160,c161 FROM 22pf to 30pf for 24M crystal accurate fail issue---SIO1184900
5.change r186 pull high to +3P3V_AUX for DDR4_DRAMRST#A and DDR4_DRAMRST#B have Glitch issue---SIO1186049
6.change c153 from 100pf reserve to 1nf install for SIO_PLTRST_N over shoot issue---SIO1185974
7.reserve D3 parallel with D24,change PS2 component far away from PS2 connector for PS2 ESD fail issue---SIO1185395

- 20150706 DC change
1.Add PJP210,PJP211,PL210
2.Add +1P35V_DUAL bleed off circuit PQ473,PR489,same as BPC.

- 20150710 DC change
1.Change DDR4 solution.DDR voltage modify,+3P3V_AUX change solution,add +VPP power

- 20150714
1.change memory schematic from DDR3L to DDR4

- 20150714 DC change
1.Change PQ960 main source to DIODES_DMP3008SFG-7

- 20150721 DC change
1.Add PR573,PC566,PQ563

Pre-SI to SI change List

- 20150812
1.PU560 change from APL5912 to APL5930

- 20150812
1.Add PCH UART circuit for kernal debug
2.Change R174,R198 to I,change R197,R193 to NI for board version change to SI
20150814
1.Add c9 100pf, change PR966 to 0ohm for SLP_S3 nmv issue---SIO1186076
2.Add c137 for SLP_S4# NMV issue---SIO1186076

- 20150818
1.PC373 change from 10nF to 33nF

SI to PV change List

- 20150923
1.Change R351to NI,R353,R354,R355,R368,R394,R105,R106,R247,R248,R222,E7 to I for PV reserve SPI recovery header and LPC debug
2.Change R193 to I,R198 to NI for board version change to PV


- 20151007
1.1.VCCIA:PR195,PR197,PR199 change from 1.37K_1% to 1.43K_1% PR174 change from 6.98K_1% to 7.32K_1%
2.VCCGT:PR101,PR103 change from 1.4K_1% to 1.43K_1% PR111 change from 17.4K_1% to 17.8K_1%
3.VCCSA:Delete PQ601_AON6934A Add PQ650_AON6594 and PQ655_AON6360
4.+1P0V_PCH:Delete PQ530_AON6934A Add PQ530_AON6594 and PQ535_AON6360

- 20151010
1.VCCSA:Add PL606_680nH_30A/20A
2.PU470,PU530,PU650 change from RT8123AGQW to NCP81230HMNTWG

PV to SMVB change List

- 20150923
1.Change R168,R197,R198to I,R196,R174,R193 to NI for board rev change to SMVB
2.change CR2,Q37,Q39,R460,R461,R463,@E16(1-2),E7,E16,R105,R106,R222,R247,R248,R353,R354,R355,R368,R394 for SMVB need remove LPC debug,bios recovery header,CR2 led

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